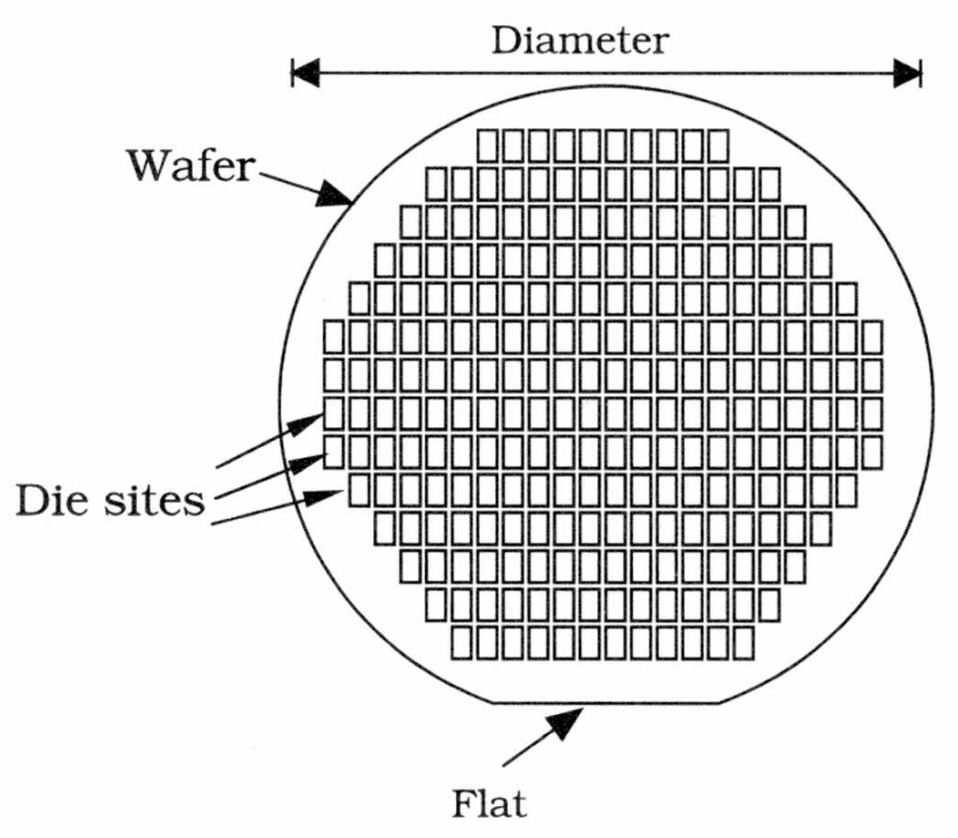
4_CMOS IC Fabrication Process

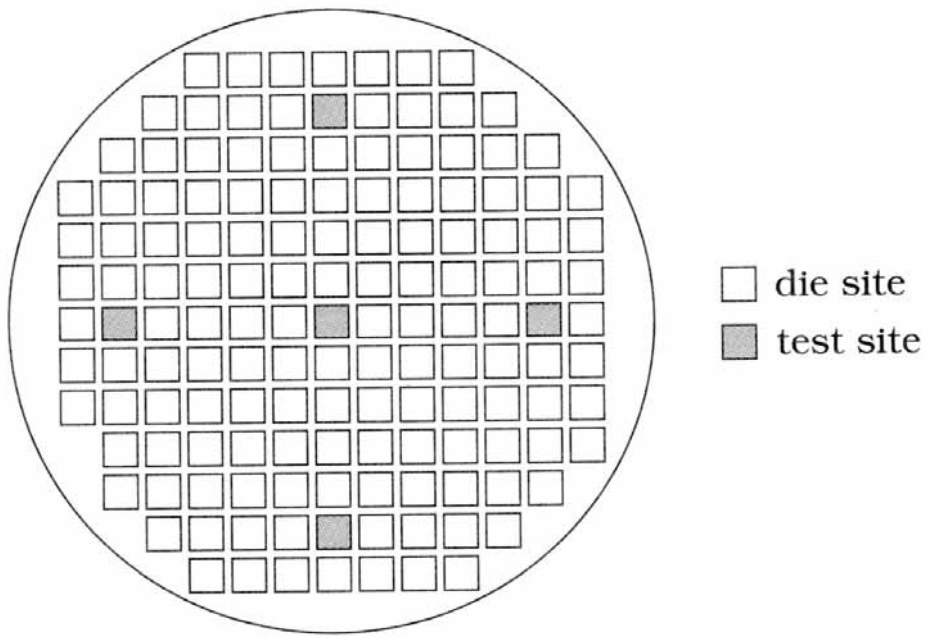
outlines

- Basic IC fabrication steps
- CMOS process steps
- Design rules

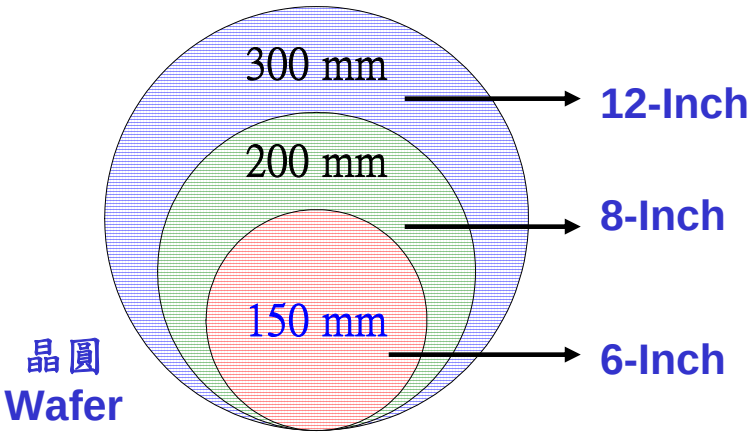
Wafer, Die, and IC

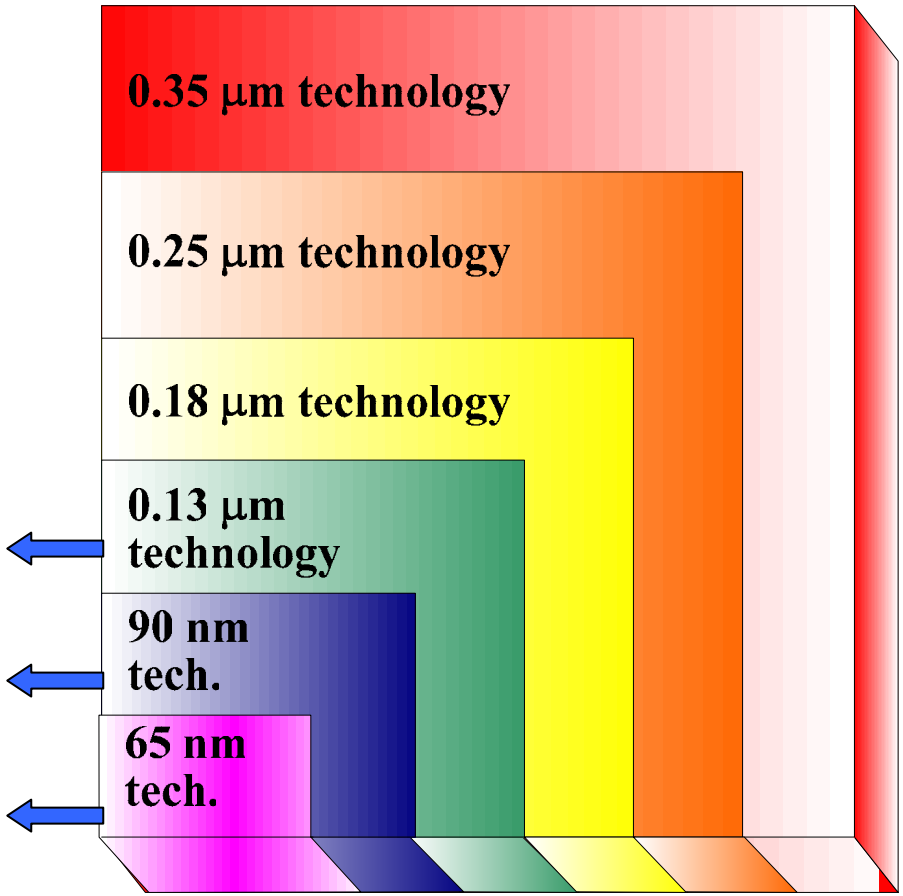
- Yield
- Defect density





目前技術的發展





和 0.18µm 製程比較

0.13µm 製程的裸晶大小約縮小 60%以上

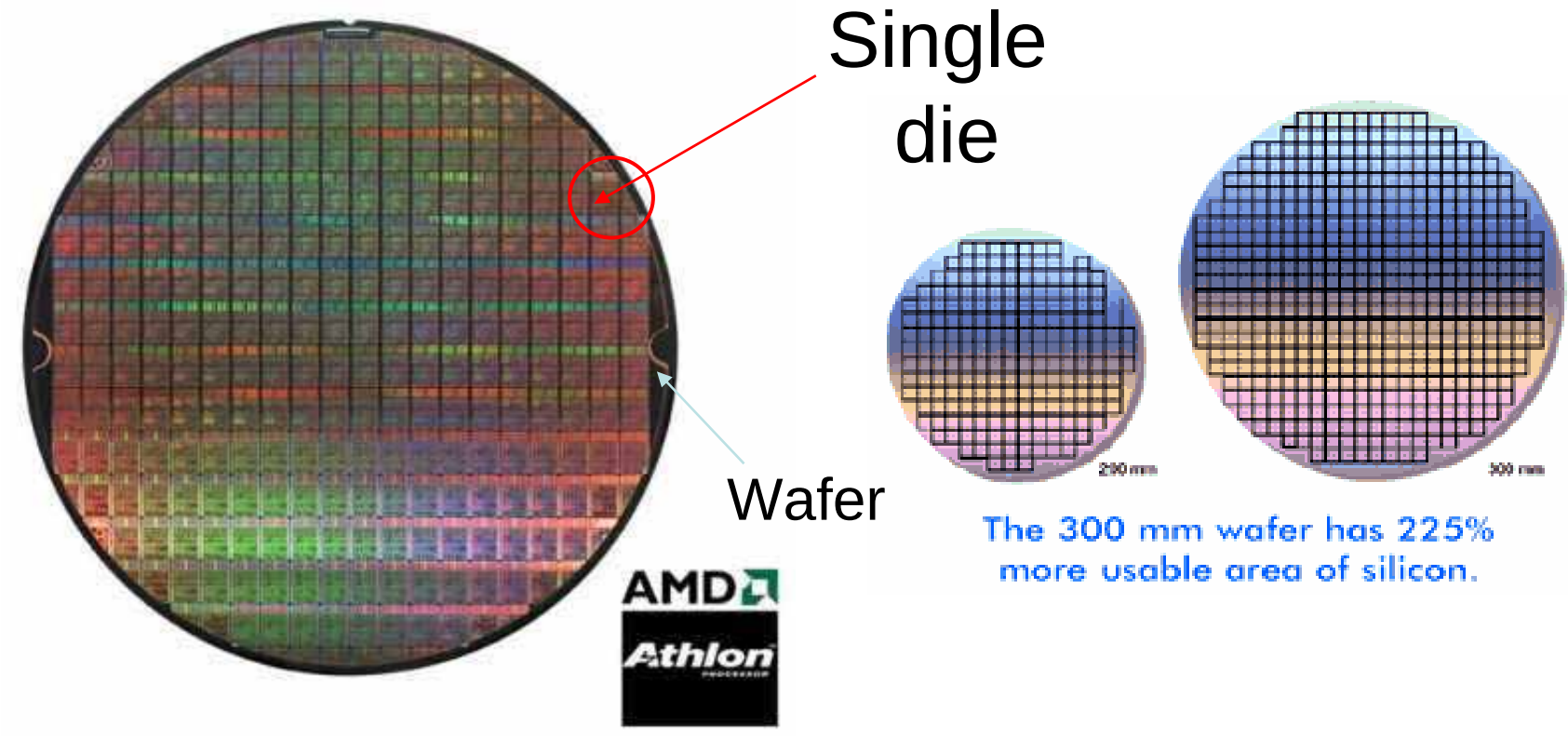
性能提昇約 70%

90-nm製程將製作在 300mm 的晶圓上

NEC 已設計出 65-nm製程所需要之 low-k薄膜技術

晶片的大小

- 晶圓的照片（Wafer photo）

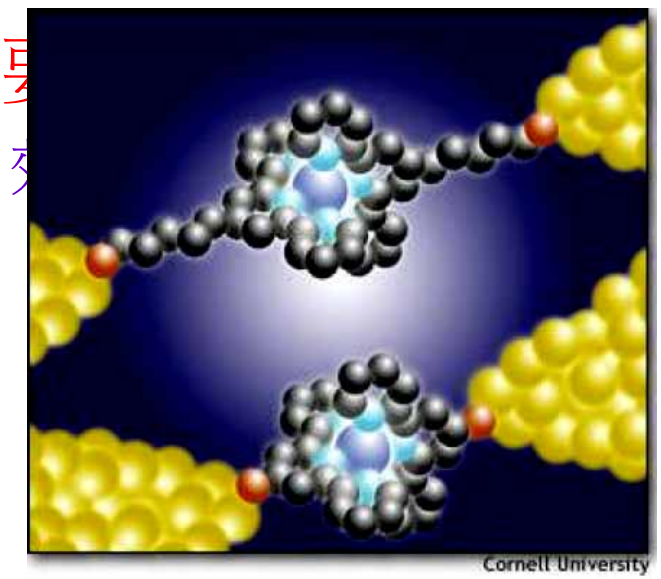


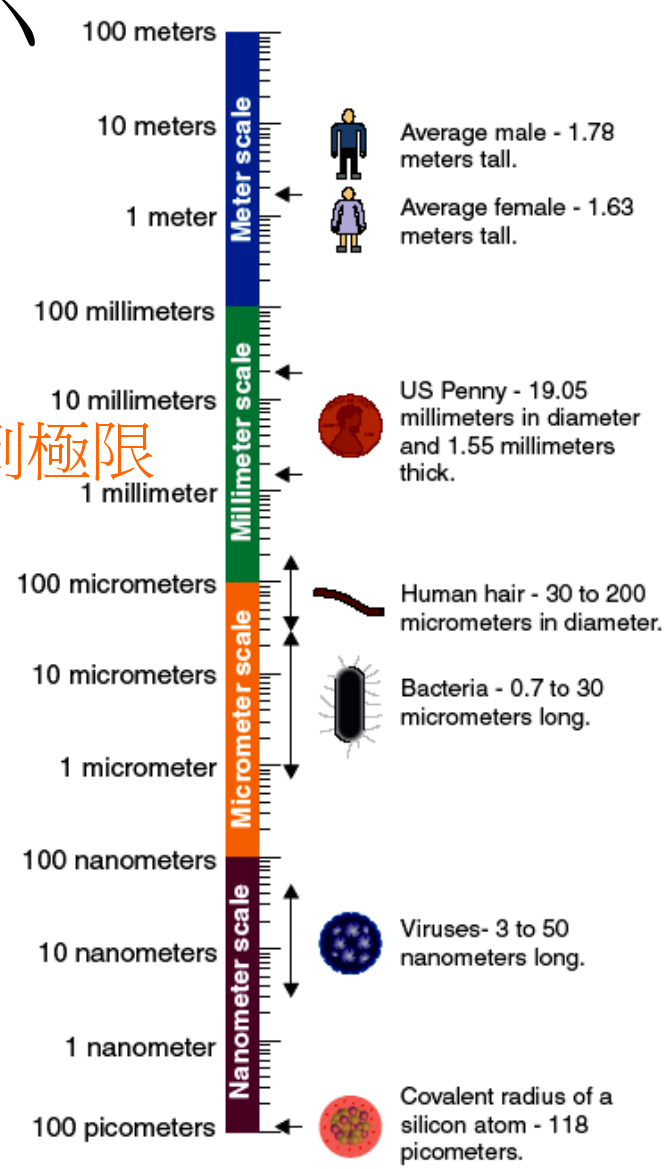
From http://www.amd.com

已提昇至 12” (30cm)

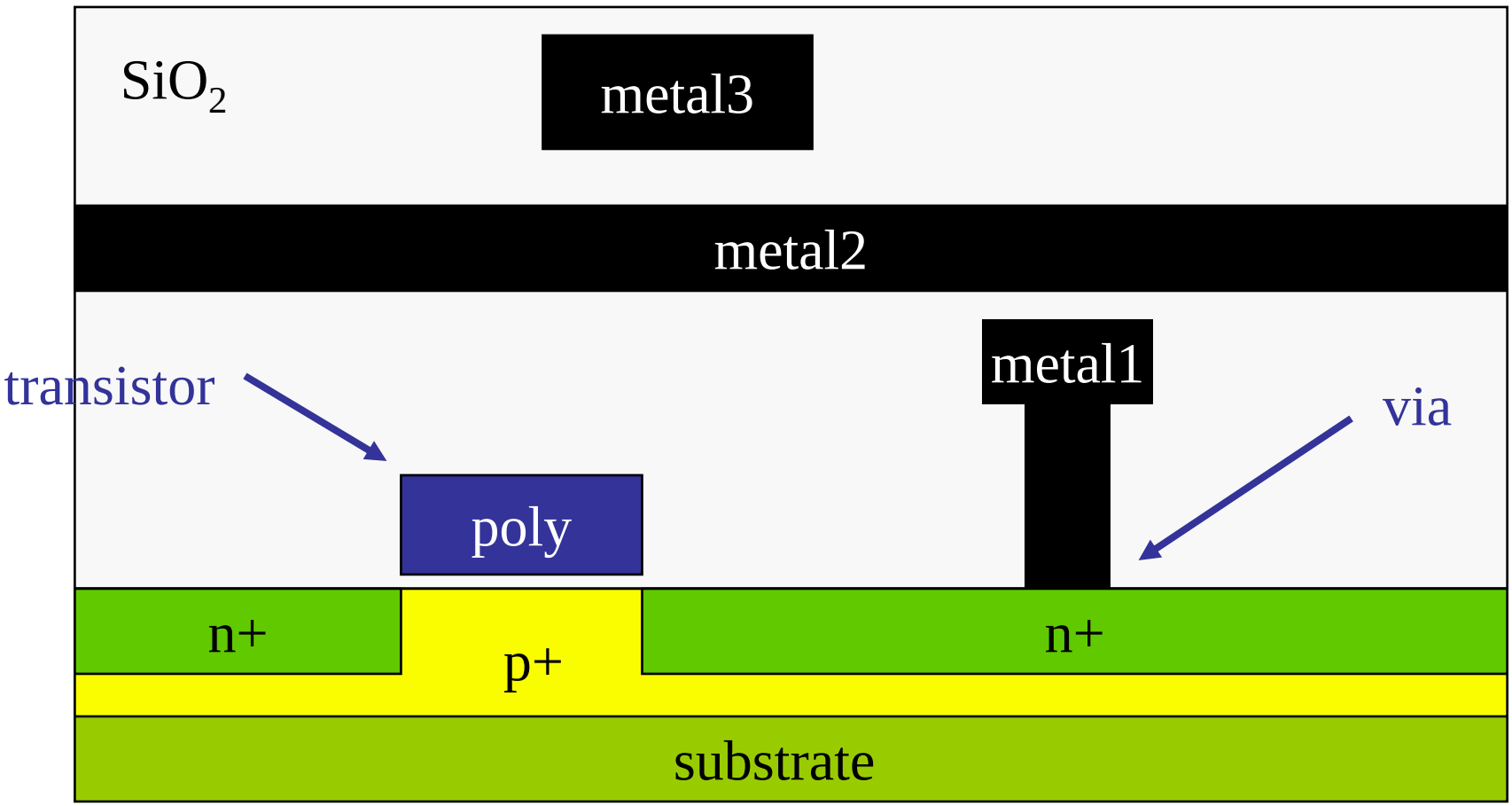
晶片的大小

- 原子的大小: 幾Å左右
  - 需要幾個原子形成一個元件
    - 似乎會在100 Å 或 0.01 μm達到極限
      - 約爲30個矽原子的大小
  - 重要
    - 交





Cross section

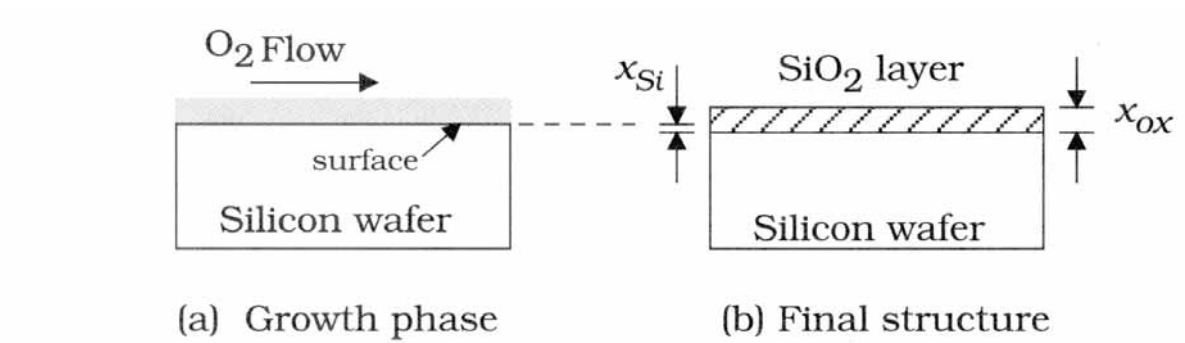


Material growth and deposition

- Oxidation
- Diffusion/ion implantation
- Polycrystal silicon
- Isolation
- Metal layers and contacts

Silicon Dioxide (SiO_2)

- Thin oxide, using dry oxidation
  - Material under the gate terminal of MOS
- Thick oxide (field oxide), using wet oxidation
  - Isolation between MOS
- CVD (chemical vapor deposition) oxide
  - Isolation between layers



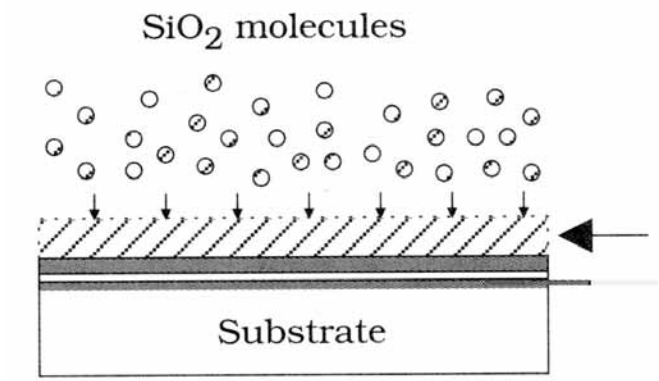


Figure 4.2 Thermal oxide growth

Doped Silicon Layers

- Diffusion of n (or p) type impurity into Si
- Ion implantation of impurity
- Form the wells in substrate
- Form the drain/source terminal of MOS

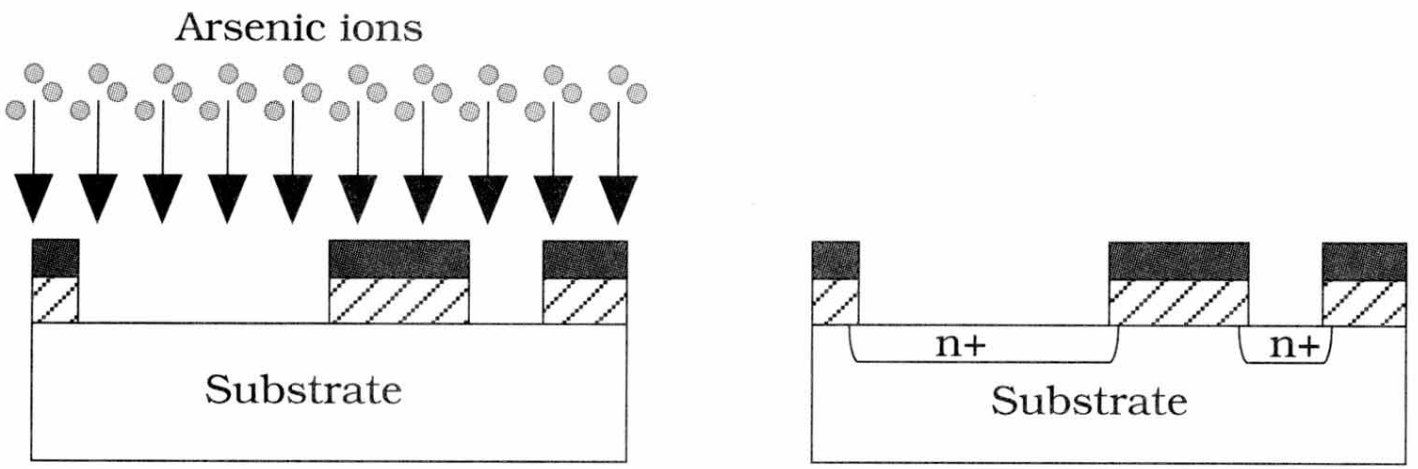


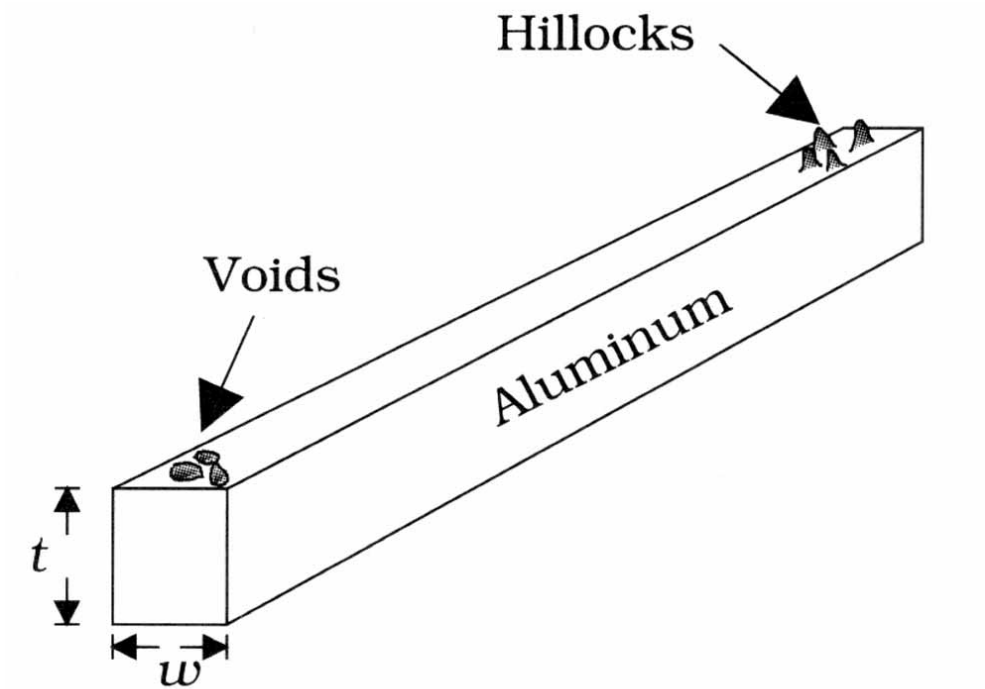
Figure 4.14 Creation of doped silicon patterns

Polysilicon

- Form gate terminal of MOS
- Originally metal gate
  - Metal Oxide Semiconductor (MOS)
- Polysilicon gate
- Silicide
  - poly coated with a thin-layer of refractory metal to reduce sheet resistance
- Can also be used in stacked capacitor for RAM process (TSMC 0.35um 2P3M)

Metal

- Aluminum (Al)
  - Material or metal layers
  - Suffers electromigration
- Copper
  - Half resistance of Al
  - Much harder process



Chemical-mechanical polishing (CMP)

- Produce planar surface using a combination of chemical etching and mechanical "sanding"
- Metal deposition steps in multi-layer metal process

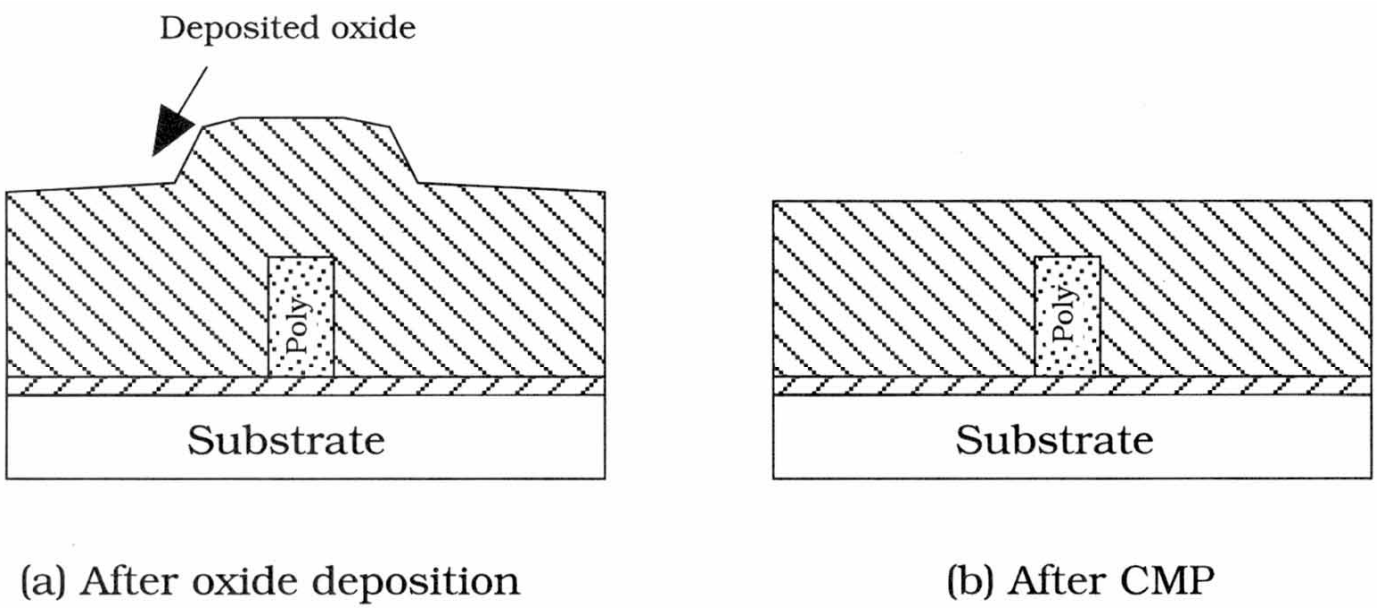


Figure 4.8 Surface planarization

Lithography (patterning)

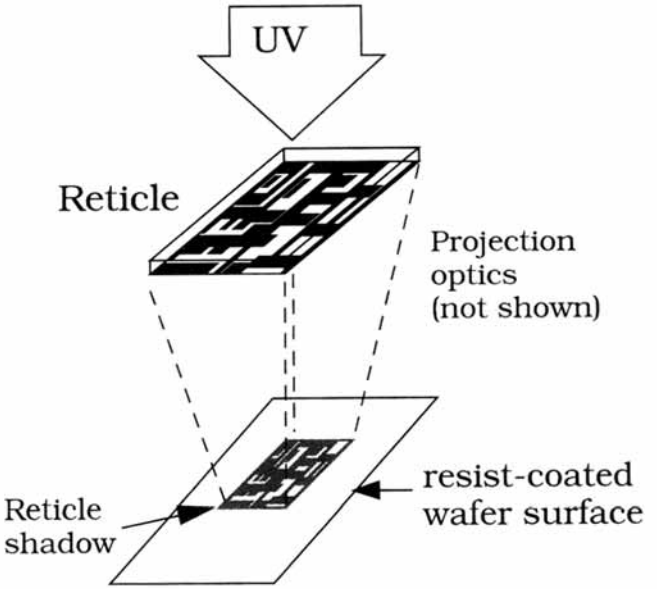
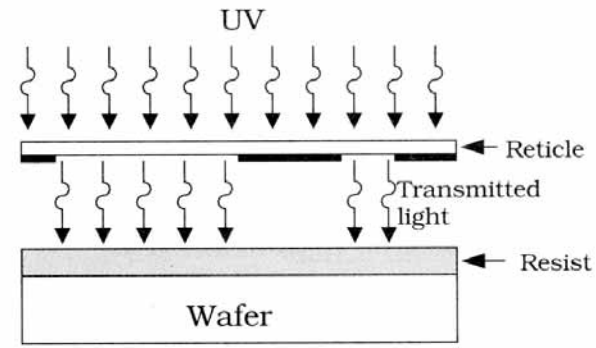
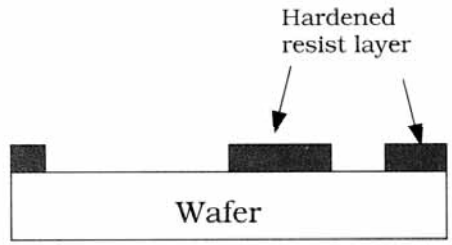


Figure 4.11 Exposure step

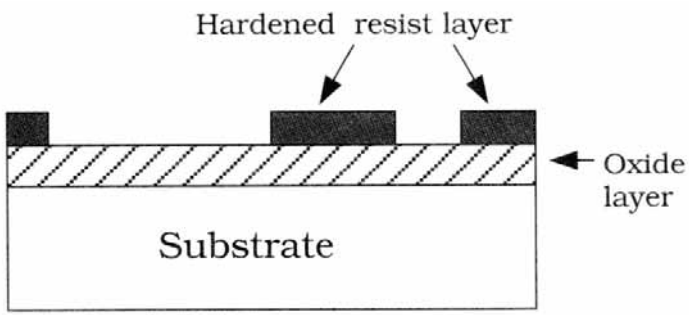


(a) Exposure pattern

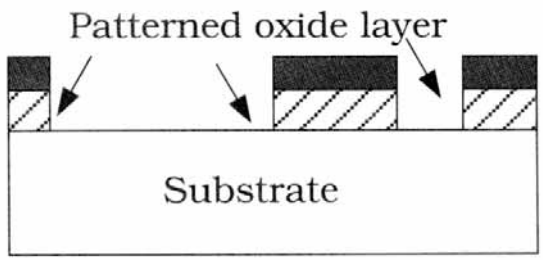


(b) After development and rinsing

Figure 4.12 Characteristics of positive photoresist



(a) Initial patterning of resist



(b) After etching process

Figure 4.13 Etching of an oxide layer

Well formation

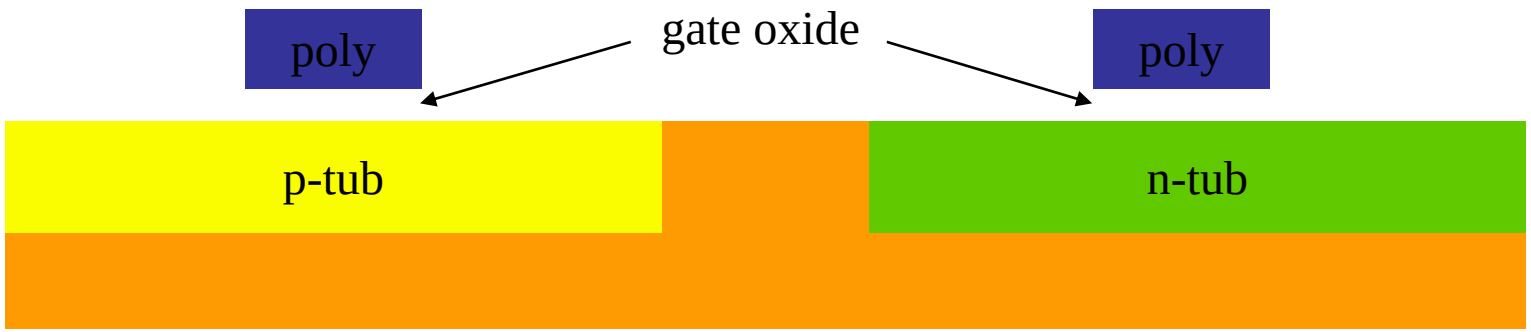
- Twin-well process

First place tubs to provide properly-doped substrate for n-type, p-type transistors:

Poly deposition

- Thin oxide (gate oxide) before poly

Pattern polysilicon before diffusion regions:



Diffusion (ion implantation)

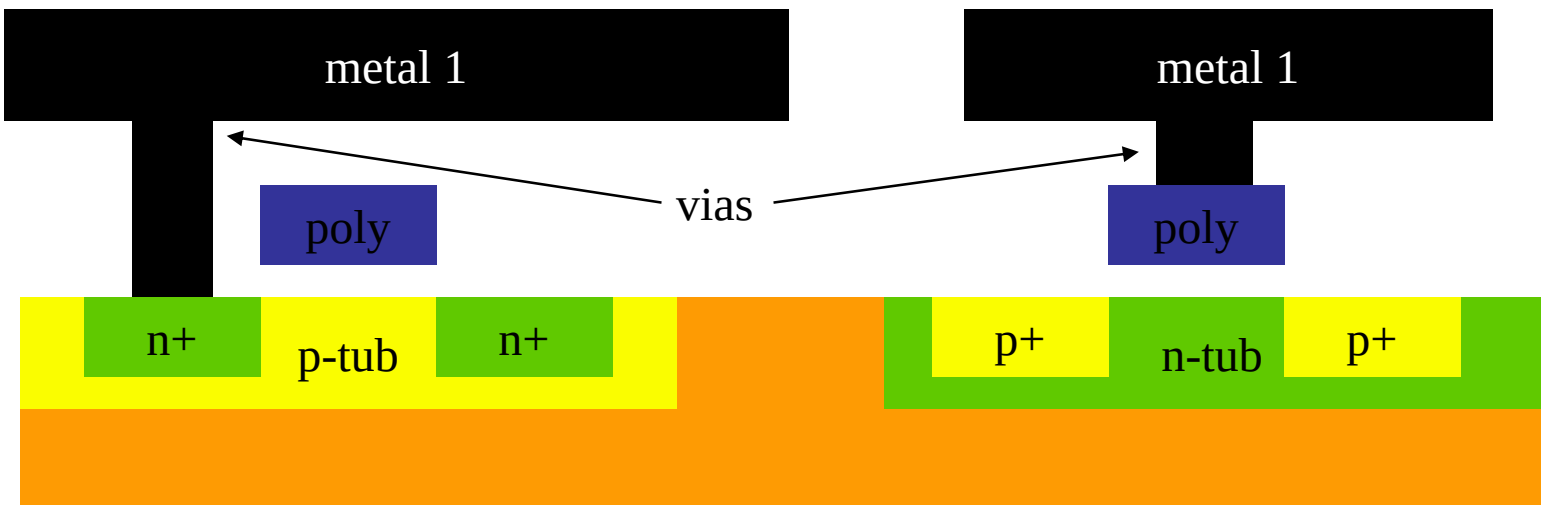
- Self-align process

Add diffusions, performing self-masking:

Metal layers and contact cuts

- Contact cuts for interconnections

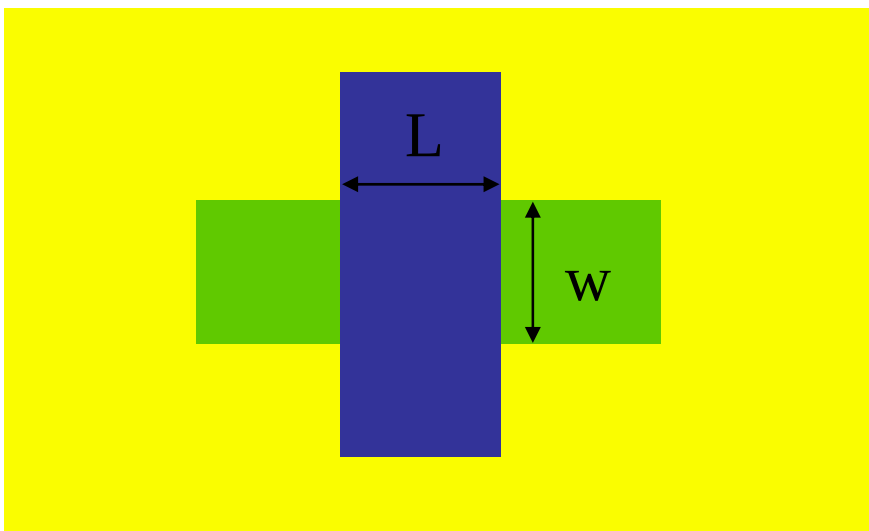
Start adding metal layers:



nMOS Transistor layout

- Length (poly width) and width (diffusion width) of MOSFET

n-type (tubs may vary):



CMOS Process I (active area)

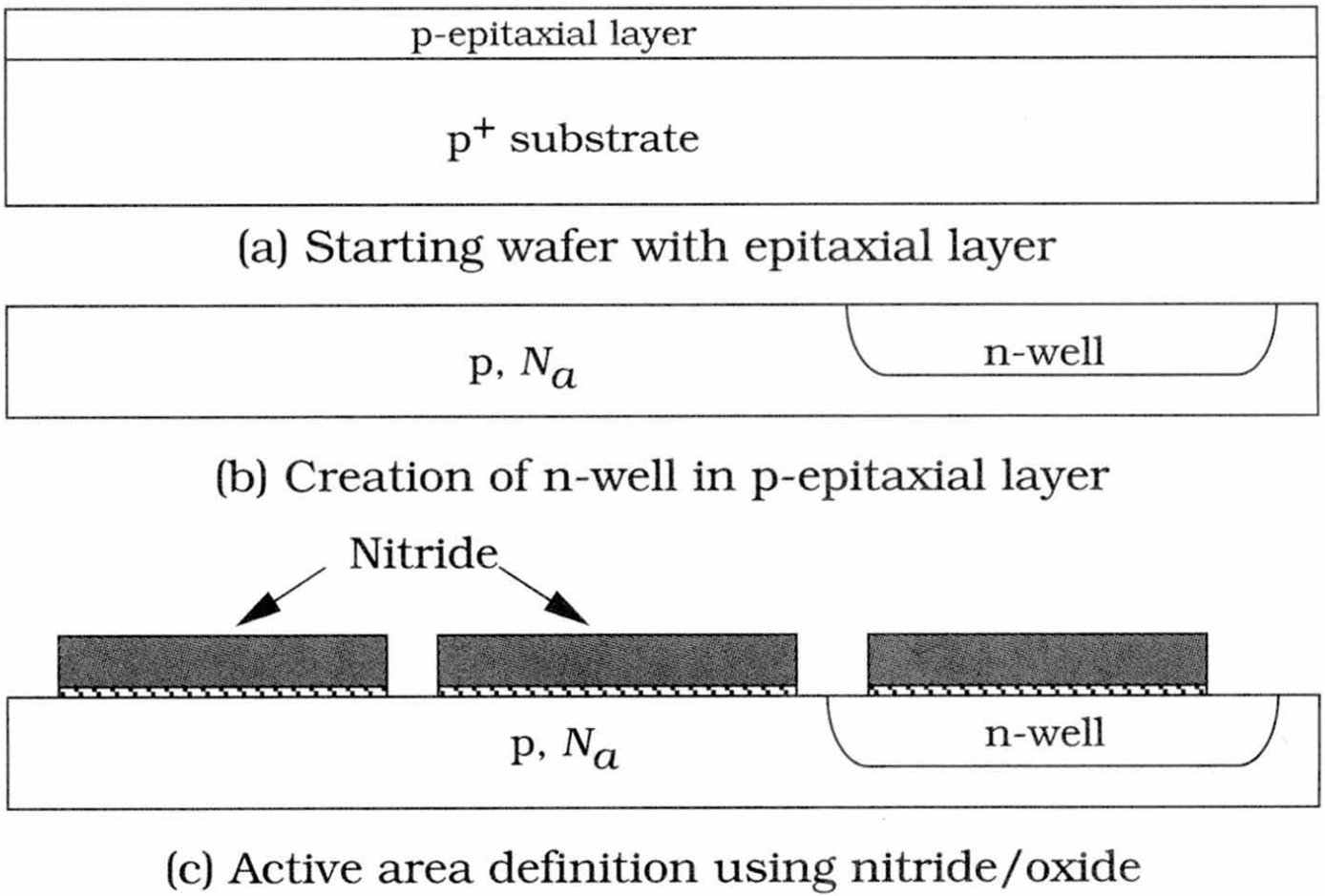


Figure 4.16 (a) Initial sequences in the CMOS fabrication sequence

CMOS process II (field oxide)

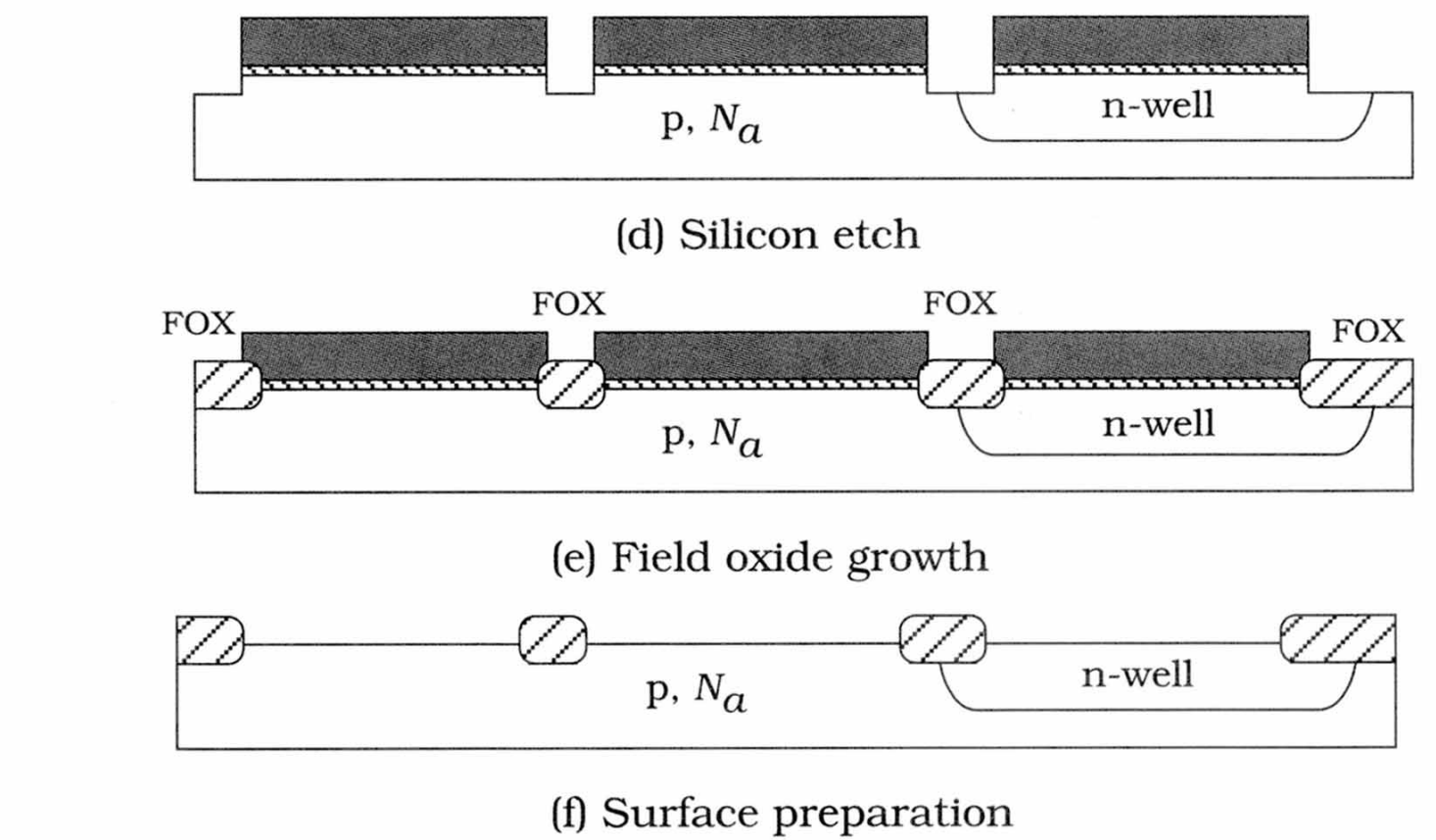
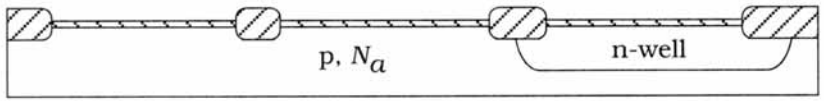
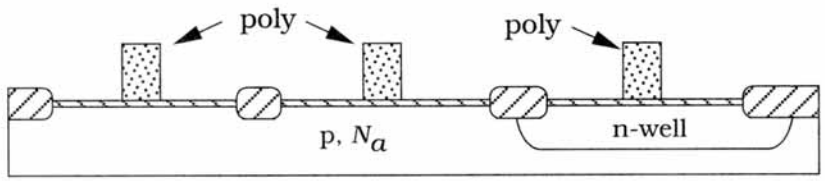


Figure 4.16(b) Initial sequences in the CMOS fabrication sequence

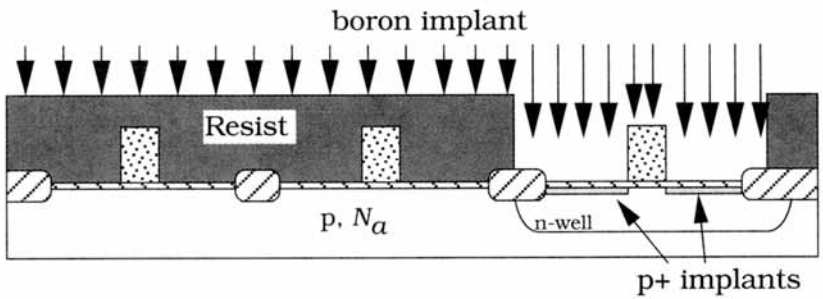
CMOS process III (MOS)



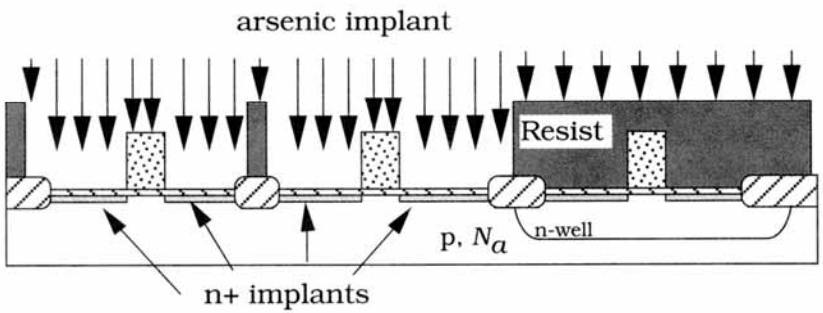
(a) Gate oxide growth



(b) Poly gate deposition and patterning



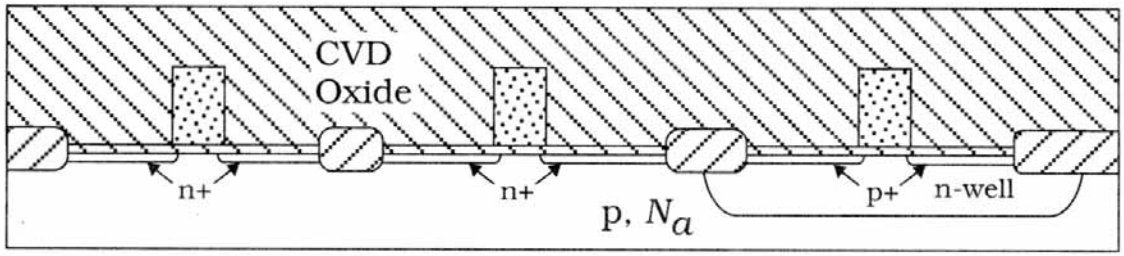
(c) pSelect mask and implant



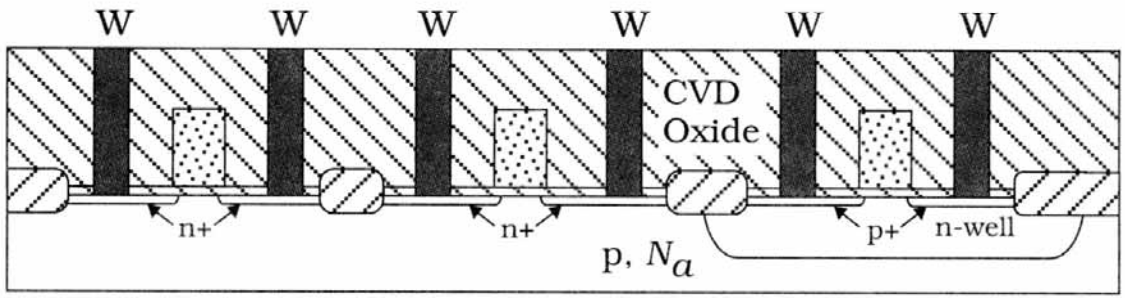
(d) nSelect mask and implant

Figure 4.17 Formation of nFETs and pFETs

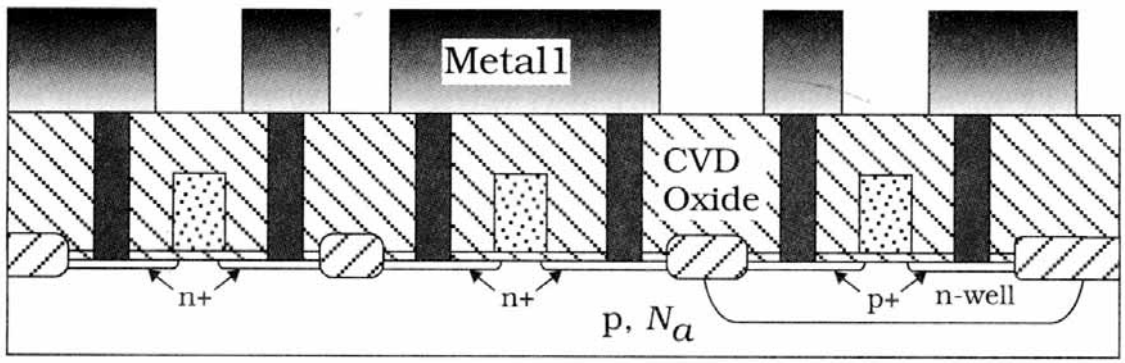
CMOS process IV (metal layer)



(a) After anneal and CVD oxide



(b) After CVD oxide active contact, W plugs



(c) Metal1 coating and patterning

Bonding pad

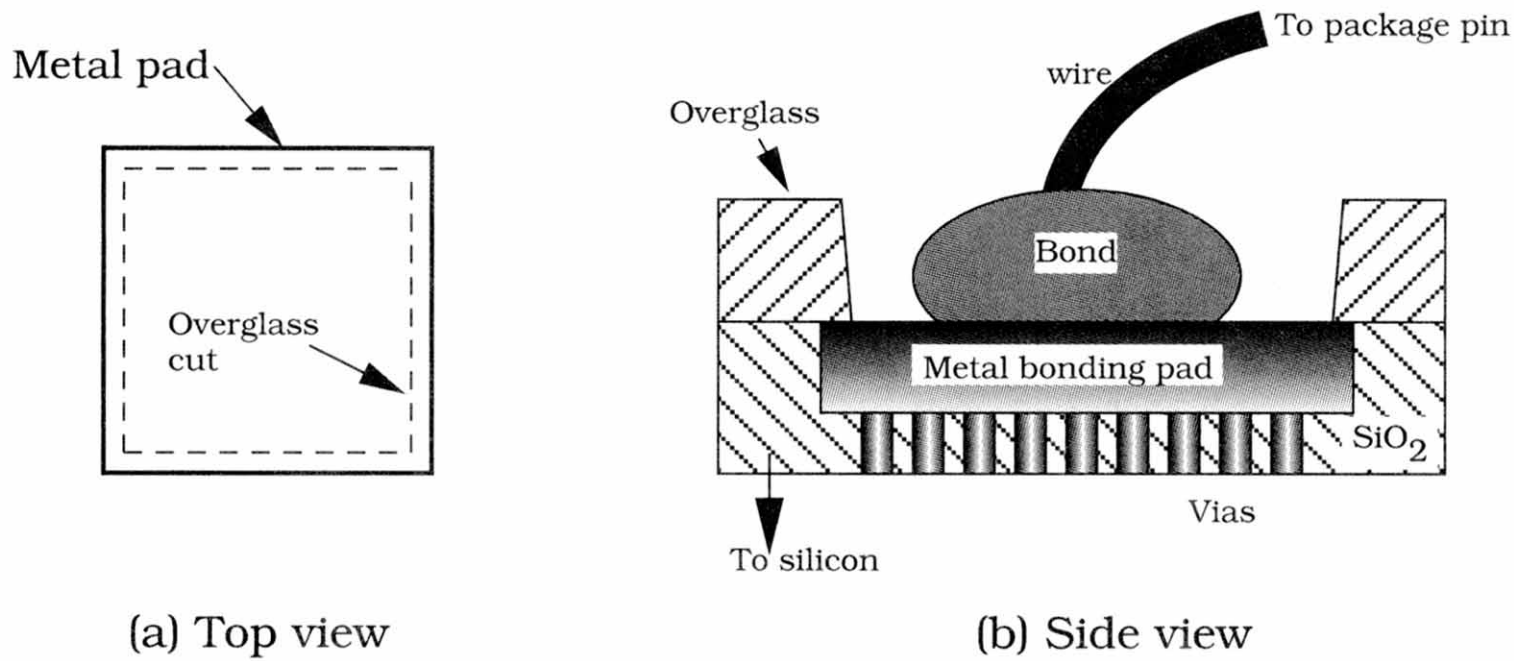
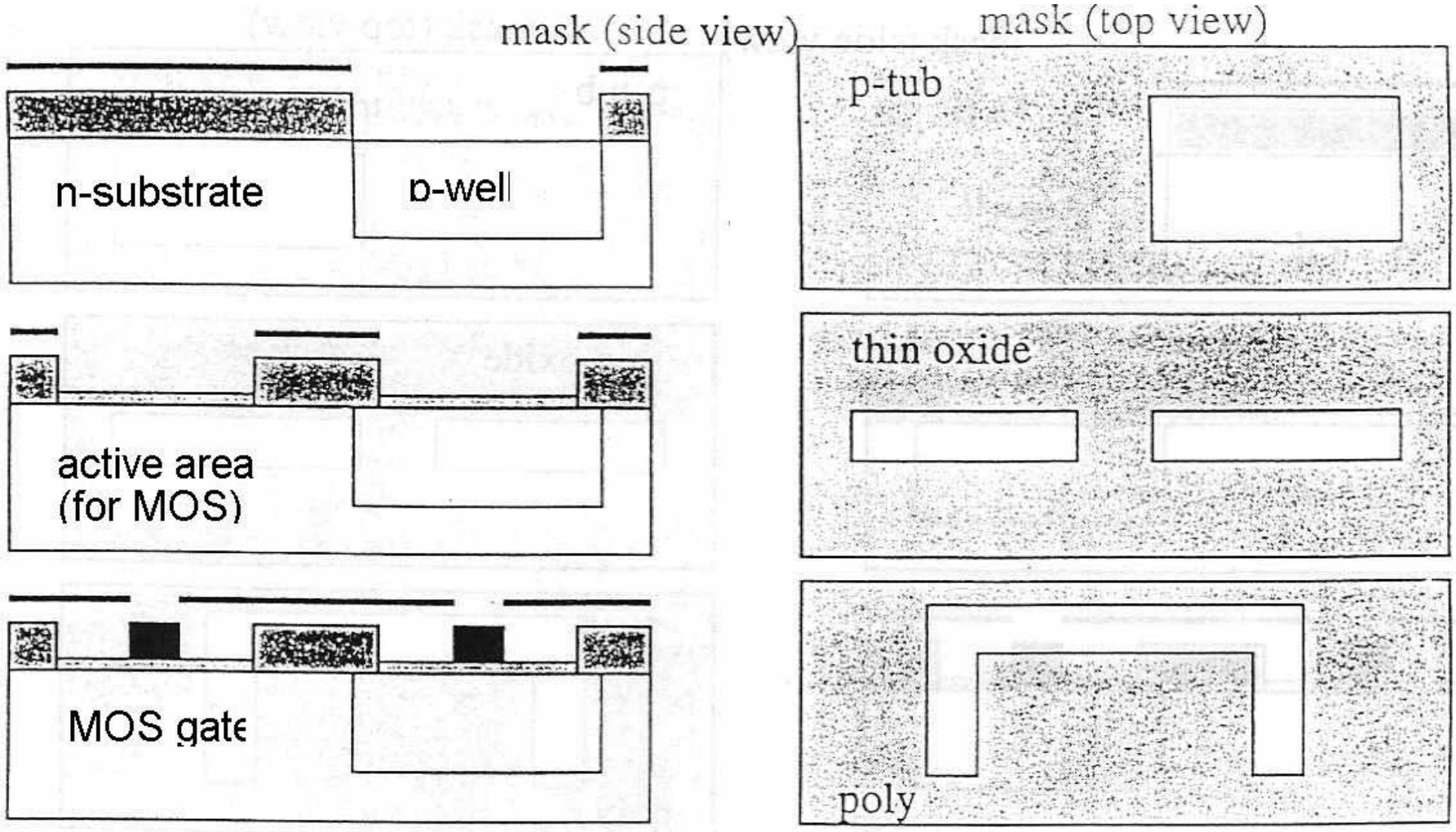
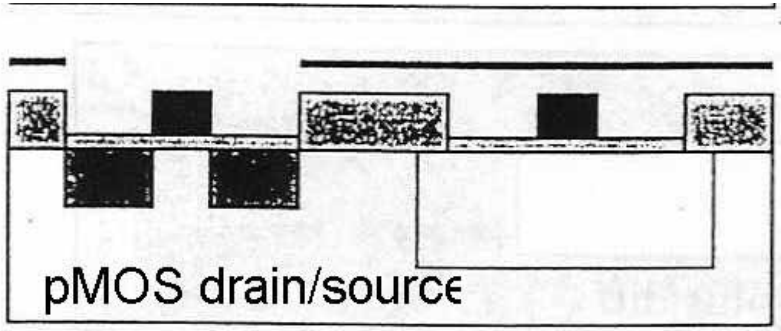


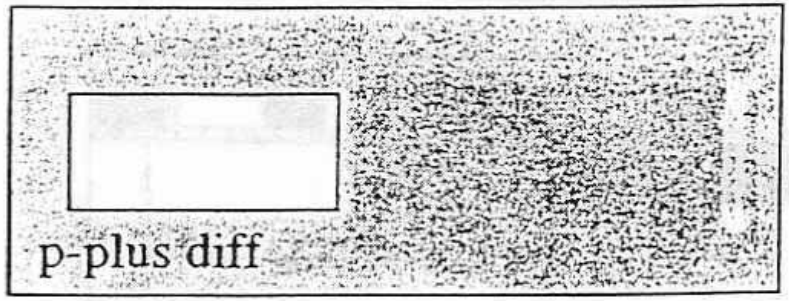
Figure 4.19 Bonding pad structure

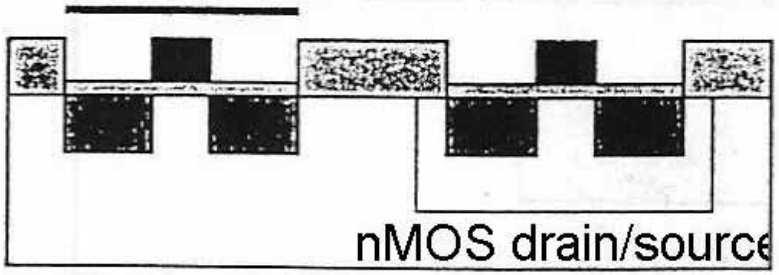
P-well CMOS: well, TOX, Poly

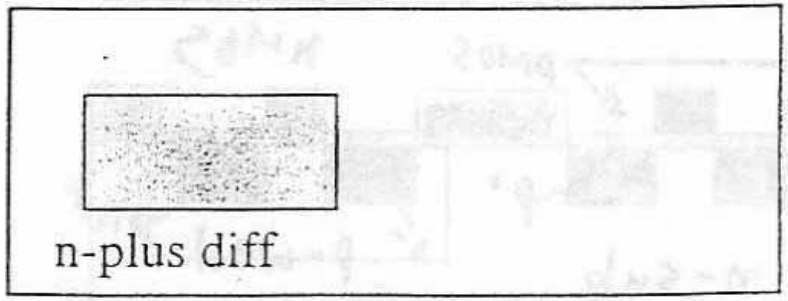


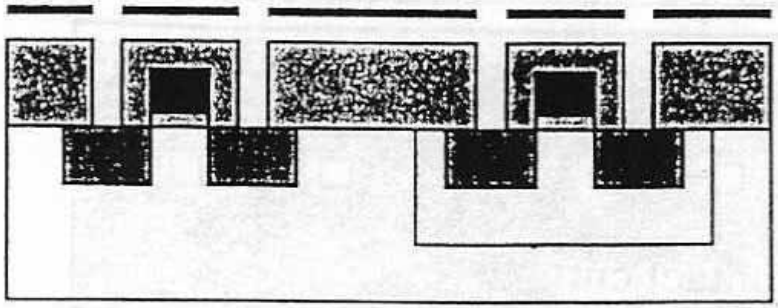
p-well CMOS: diff, cut, metal

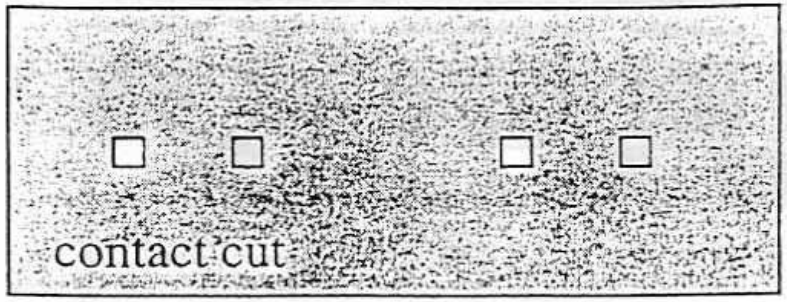


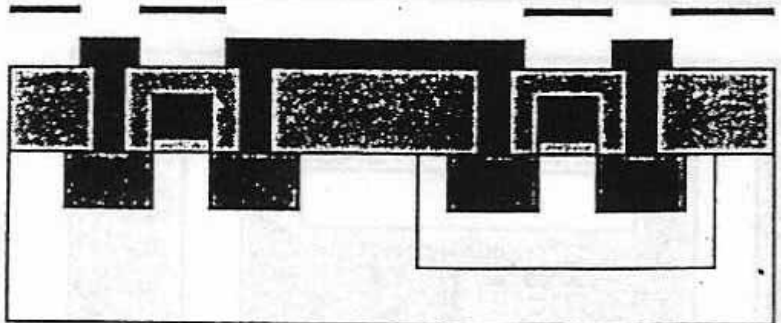


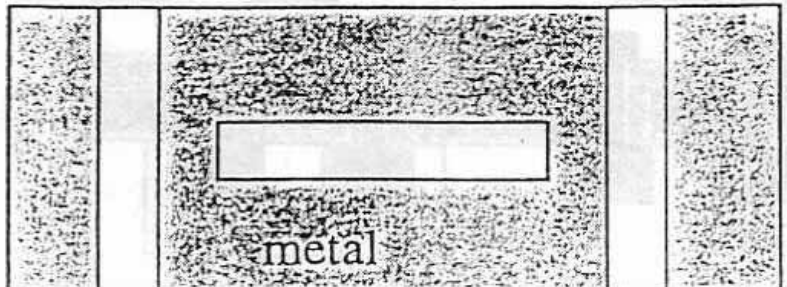






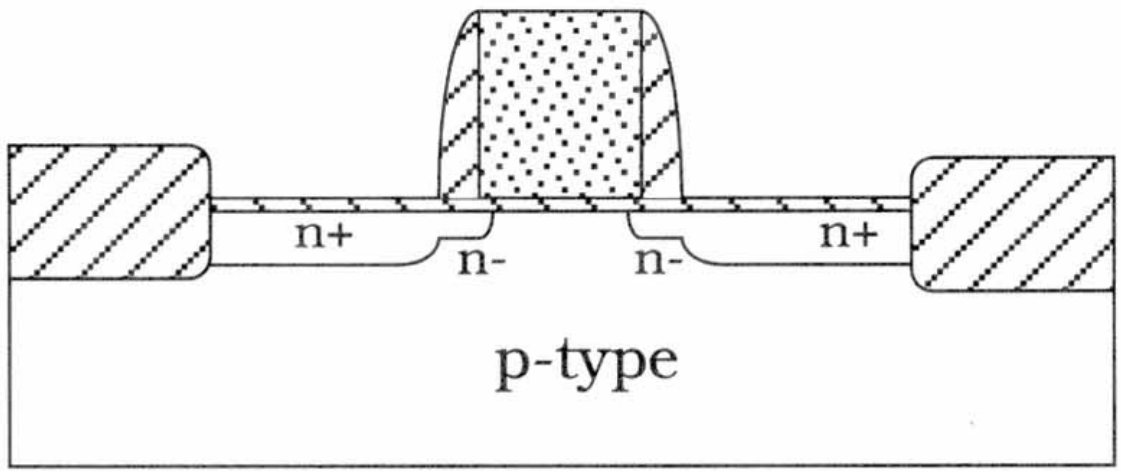






Lightly doped drain (LDD)

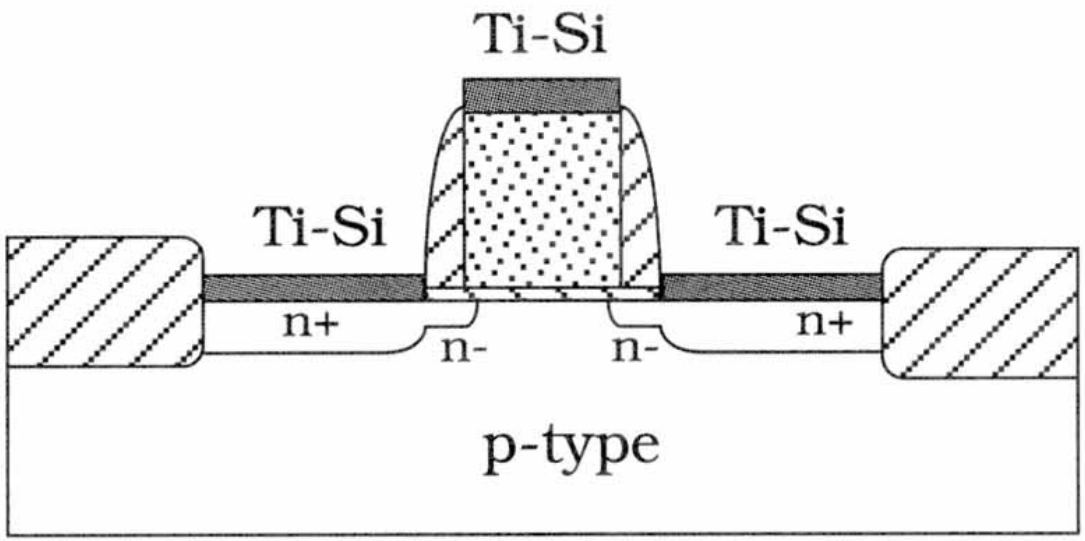
- Reduce hot-electron effects in short-channel devices
- Transparent to layout designers



(a) LDD FET structure

Silicide

- Even heavily doped polysilicon has large sheet resistance (about 25 ohm)
- Add refactory metal to reduce the sheet resistance to about 10m ohm



(b) Silicide formation

Copper patterning

- Half resistance of Al
- Hard to etch
- Diffuse rapidly through Si
- Damascene process

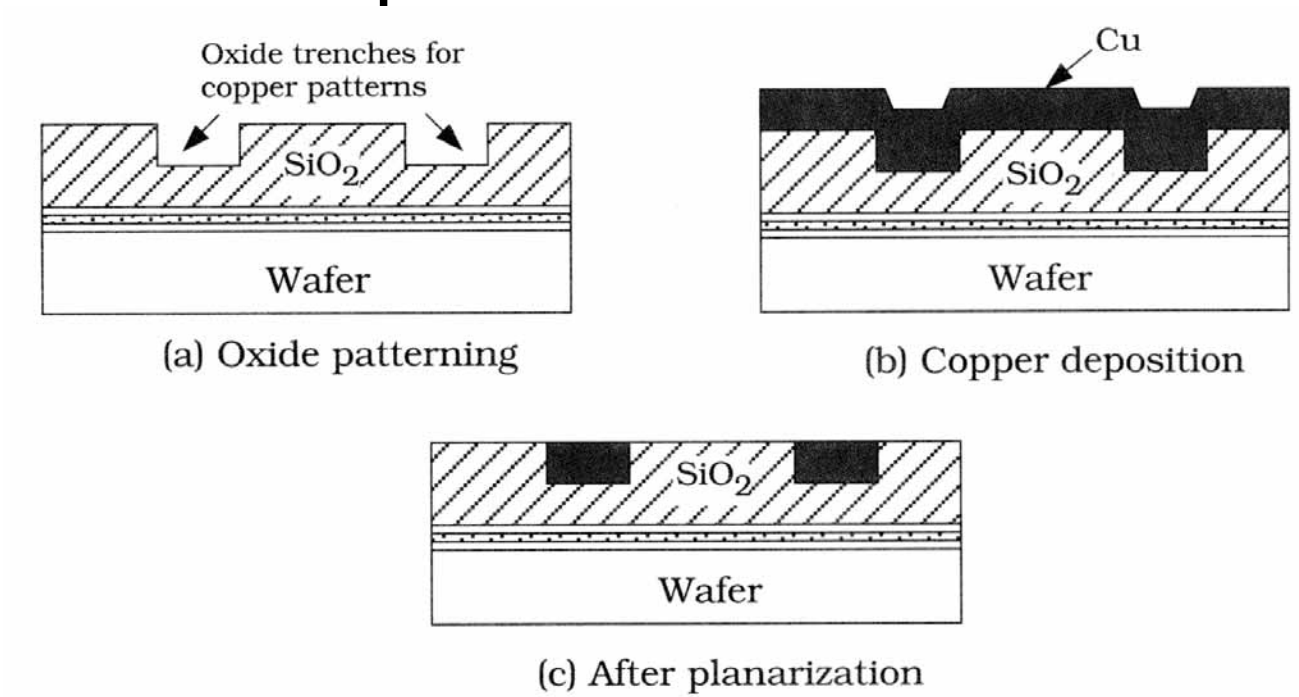


Figure 4.22 Copper patterning using the Damascene process

Dual-Damascene for Cu

- Create via using Cu
- Thin barrier layers are required to contain Cu

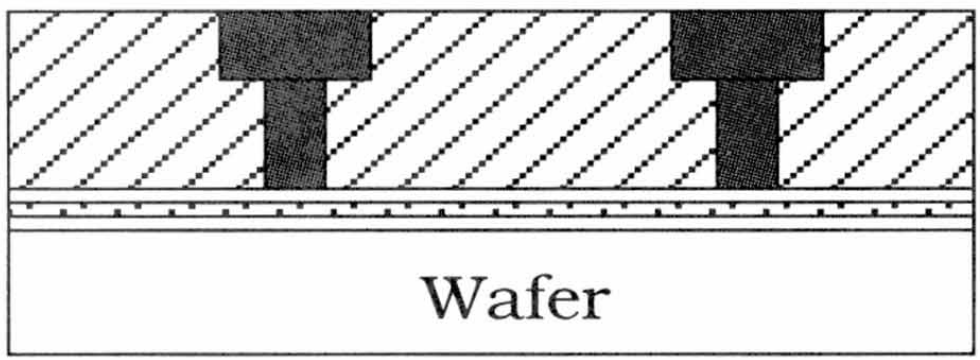


Figure 4.23 Dual-Damascene structure with copper vias

Design rules

- Minimum dimension, line spacing, overlapping, extension of different patterns
- Micron rules
  - Unit of micron meters
  - Technology dependent (non-scalable)
- Lambda rules
  - Unit of lambda
  - Technology independent (scalable)

Design rules

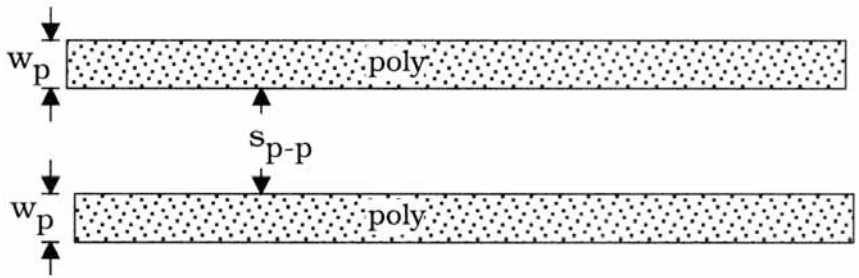
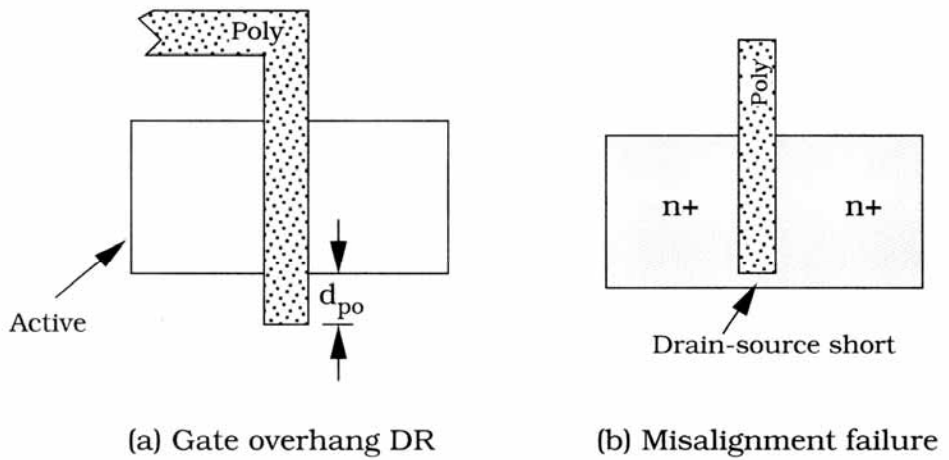
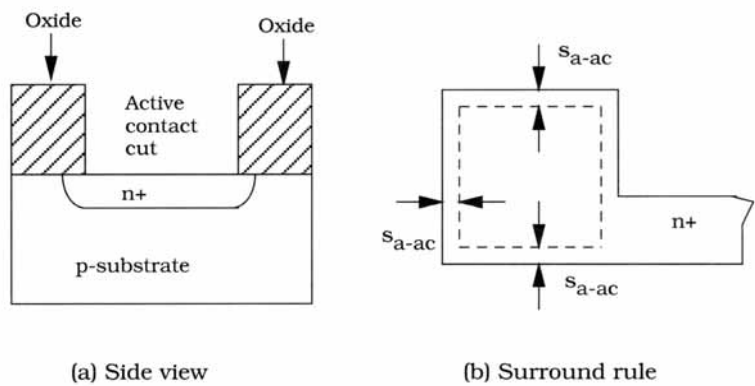


Figure 4.24 Design rule limits for two polysilicon lines



(a) Gate overhang DR (b) Misalignment failure

Figure 4.27 Example of an extend (gate overhang) design rule



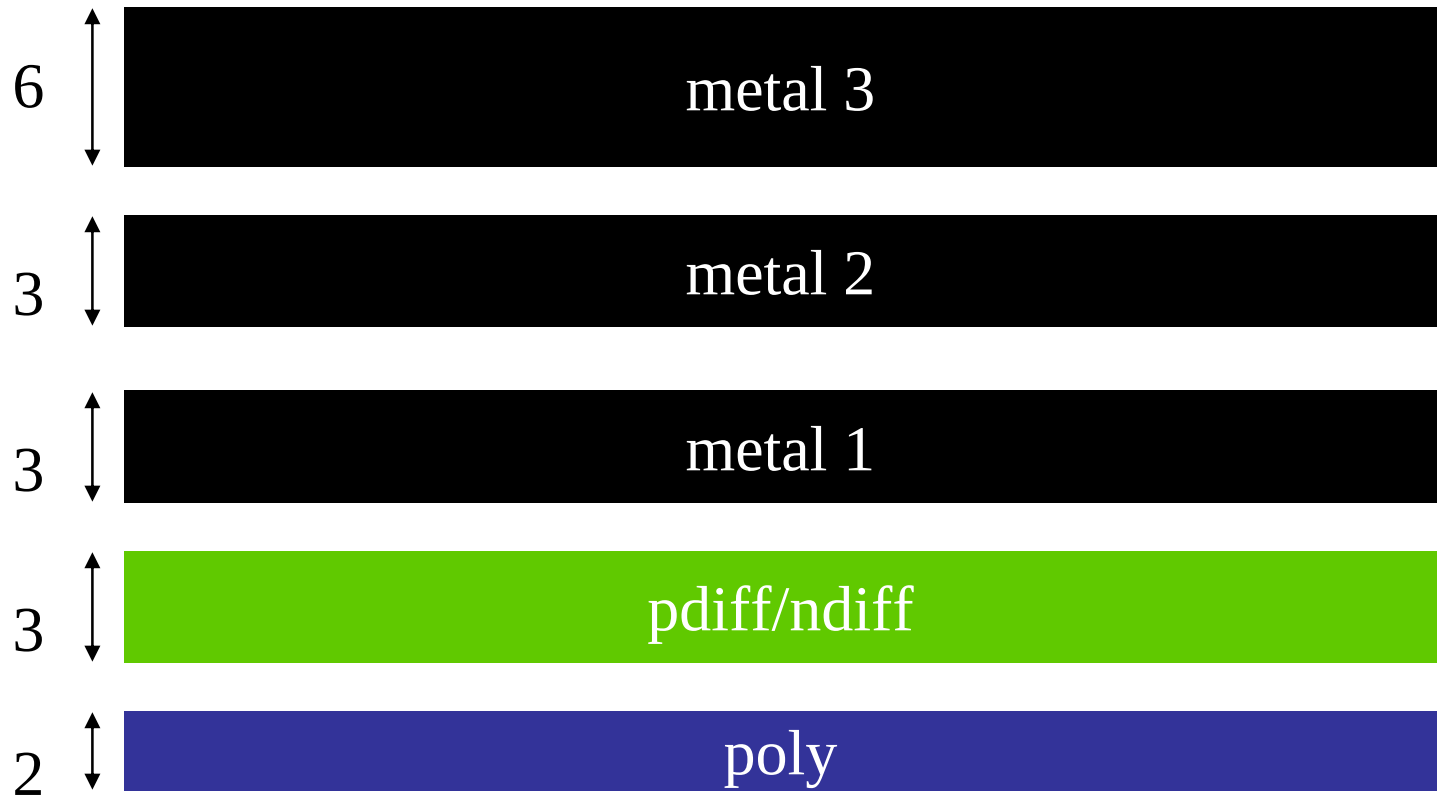
(a) Side view (b) Surround rule

Figure 4.25 Example of a surround design rule

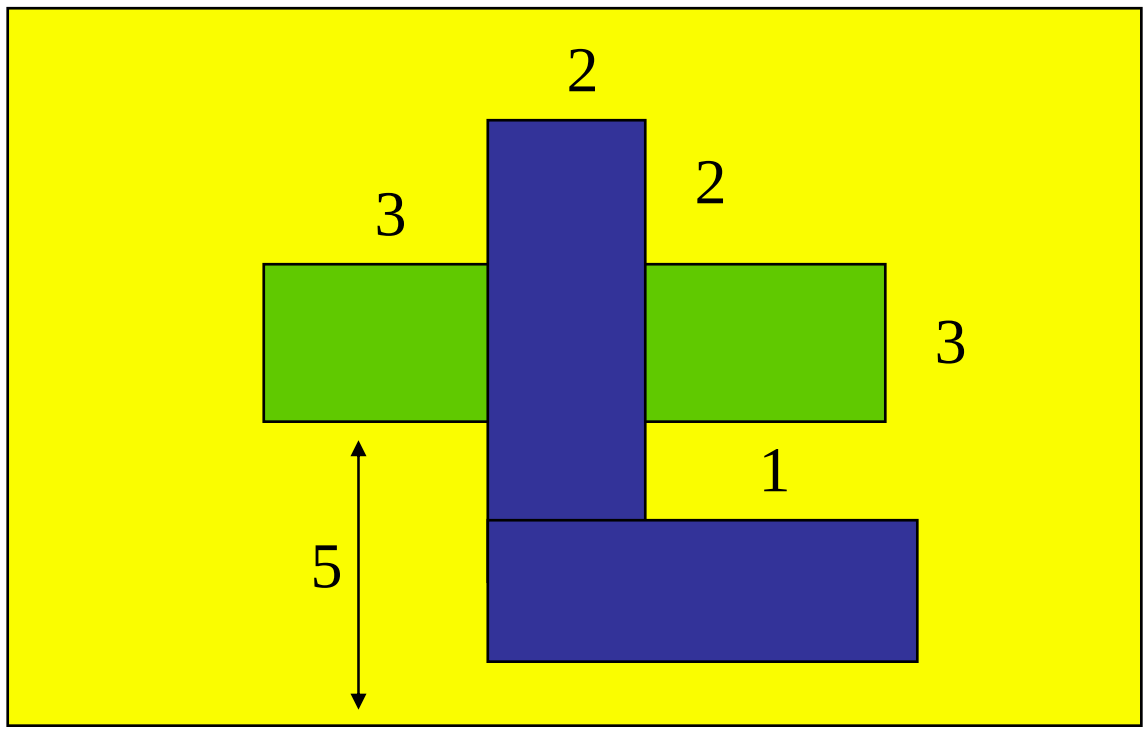
MOSIS scalable lambda rules

- Designed to scale across a wide range of technologies
- Designed for educational use
- fairly conservative
- λ is the size of a minimum feature.
- Specifying λ particularizes the scalable rules.
- Parasitics are generally not specified in λ units.

wires

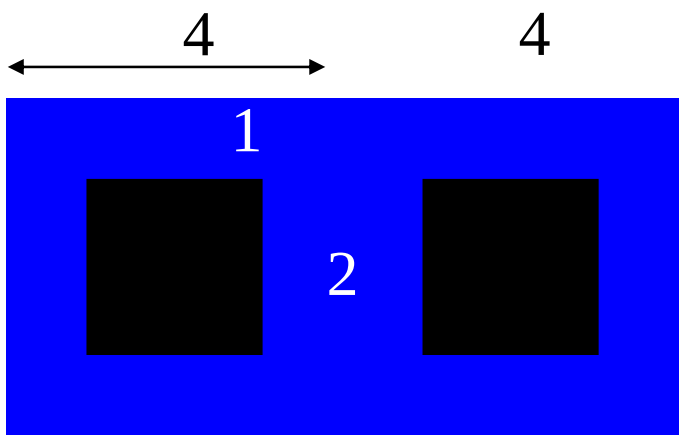


transistors



vias

- Types of via: metal1/diff, metal1/poly, metal1/metal2.

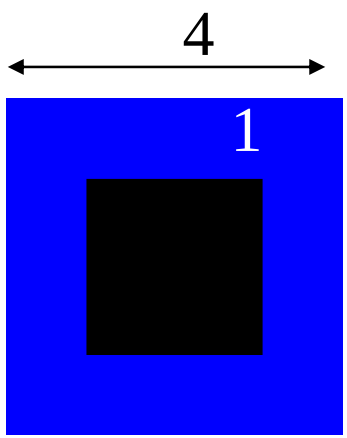


Metal 3 vias

- Type: metal3/metal2.
- Rules:
  - cut: 3 x 3
  - overlap by metal2: 1
  - minimum spacing: 3
  - minimum spacing to via1: 2

Tub ties

- Also called Substract contact (or well contact)



spacings

- Diffusion/diffusion: 3
- Poly/poly: 2
- Poly/diffusion: 1
- Via/via: 2
- Metal1/metal1: 3
- Metal2/metal2: 4
- Metal3/metal3: 4

overglass

- Cut in passivation layer.
- Minimum bonding pad: 100 m.
- Pad overlap of glass opening: 6
- Minimum pad spacing to unrelated metal2/3: 30
- Minimum pad spacing to unrelated metal1, poly, active: 15

SCMOS Design Rules

- Scalable CMOS (SCMOS) design rules
  - Technology independent (unit of lambda)
  - Standard (1.5um – 0.35um)
  - SUBM (0.5um – 0.18um)
  - DEEP (0.25um – 0.18um)
- Layers
  - Well (n-well, p-well, twin-well)
  - Active (thin oxide)
  - Poly
  - Contact to Poly and Active
  - Via to Metal

Standard MOSIS SCMOS (1.5um – 0.35um)

Table 2a: MOSIS SCMOS-Compatible Mappings

Foundry	Process	Lambda (micrometers)	Options
AMI	ABN (1.5 micron *n*-well)	0.80	SCNA, SCNE
AMI	C5N (0.5 micron *n*-well)	0.35	SCN3M, SCN3ME
Agilent/HP	AMOS14TB (0.5 micron *n*-well)	0.35	SCN3M, SCN3MLC
TSMC	0.35 micron 2P4M (4 Metal Polycided, 3.3 V/5 V)	0.25	SCN4ME
TSMC	0.35 micron 1P4M (4 Metal Silicided, 3.3 V/5 V)	0.25	SCN4M

SUBM (Submicron)
0.5um – 0.18um

Table 2b: MOSIS SCMOS_SUBM-Compatible Mappings

Foundry	Process	Lambda (micrometers)	Options
AMI	C5N (0.5 micron *n*-well)	0.30	SCN3M_SUBM, SCN3ME_SUBM
Agilent/HP	AMOS14TB (0.5 micron *n*-well)	0.30	SCN3M_SUBM, SCN3MLC_SUBM
TSMC	0.35 micron 2P4M (4 Metal Polycided, 3.3 V/5 V)	0.20	SCN4ME_SUBM
TSMC	0.35 micron 1P4M (4 Metal Silicided, 3.3 V/5 V)	0.20	SCN4M_SUBM
TSMC	0.25 micron 5 Metal 1 Poly (2.5 V/3.3 V)	0.15	SCN5M_SUBM
TSMC	0.18 micron 6 Metal 1 Poly (1.8 V/3.3 V)	0.10	SCN6M_SUBM

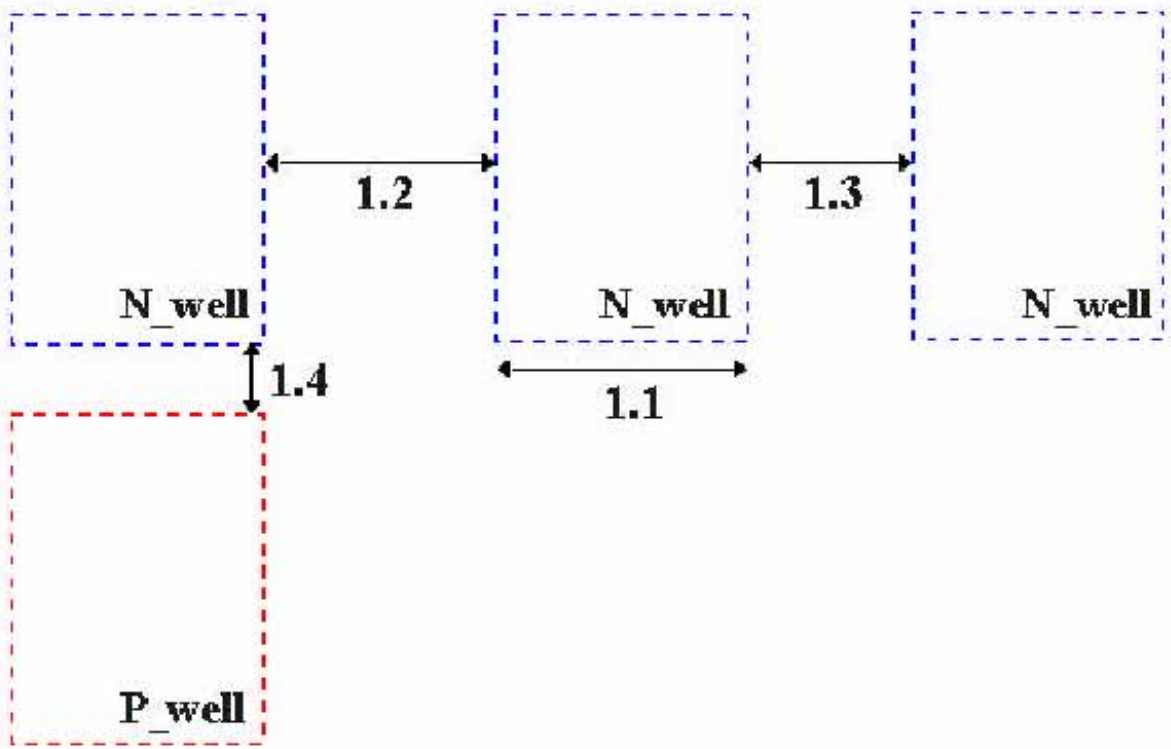
DEEP (deep submicron) 0.25um – 0.18um

Table 2c: MOSIS SCMOS_DEEP-Compatible Mappings

Foundry	Process	Lambda (micrometers)	Options
TSMC	0.25 micron 5 Metal 1 Poly (2.5 V/3.3 V)	0.12	SCN5M_DEEP
TSMC	0.18 micron 6 Metal 1 Poly (1.8 V/3.3 V)	0.09	SCN6M_DEEP

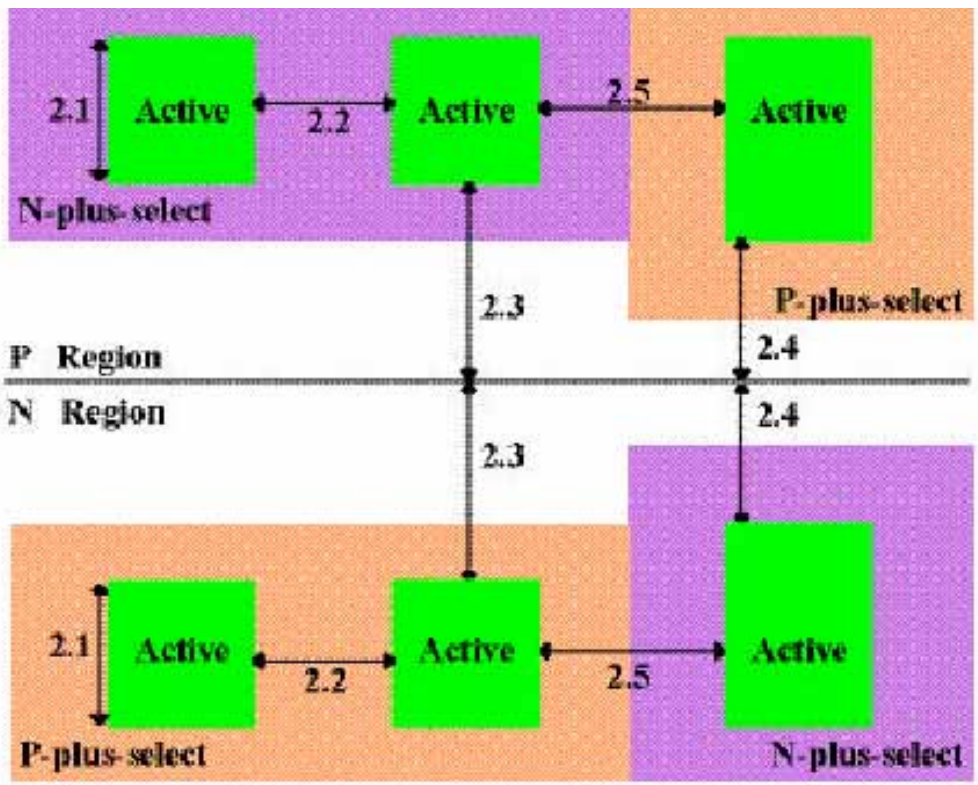
Well

Rule	Description	Lambda		
		SCMOS	SUBM	DEEP
1.1	Minimum width	10	12	12
1.2	Minimum spacing between wells at different potential	9	18	18
1.3	Minimum spacing between wells at same potential	6	6	6
1.4	Minimum spacing between wells of different type (if both are drawn)	0	0	0



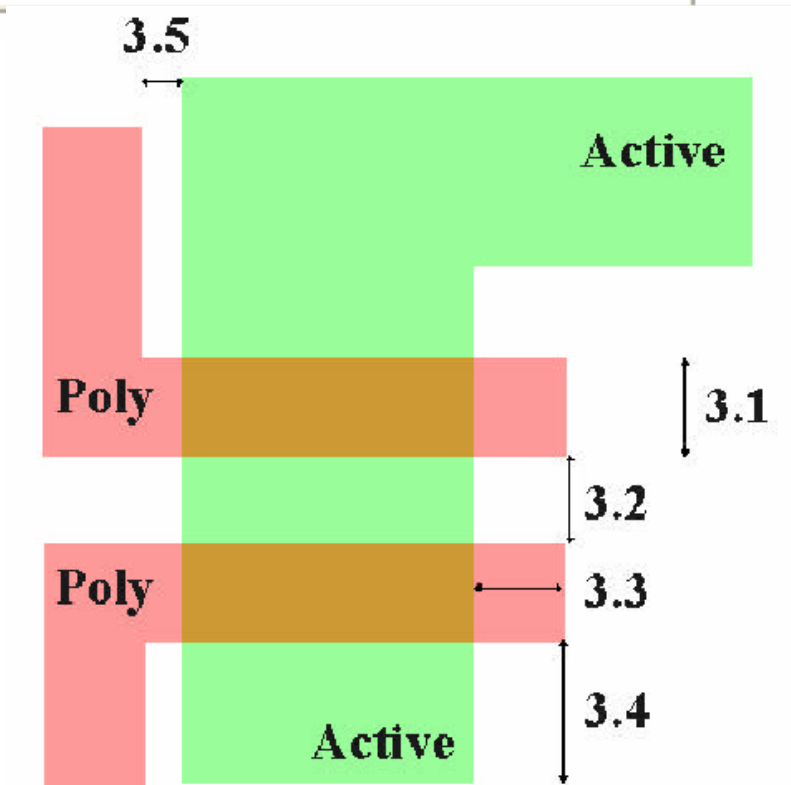
Active (MOS transistor area)

Rule	Description	Lambda		
		SCMOS	SUBM	DEEP
2.1	Minimum width	3 *	3 *	3
2.2	Minimum spacing	3	3	3
2.3	Source/drain active to well edge	5	6	6
2.4	Substrate/well contact active to well edge	3	3	3
2.5	Minimum spacing between non-abutting active of different implant. Abutting active ("split-active") is illustrated under Select Layout Rules.	4	4	4



Poly (gate terminal of MOS)

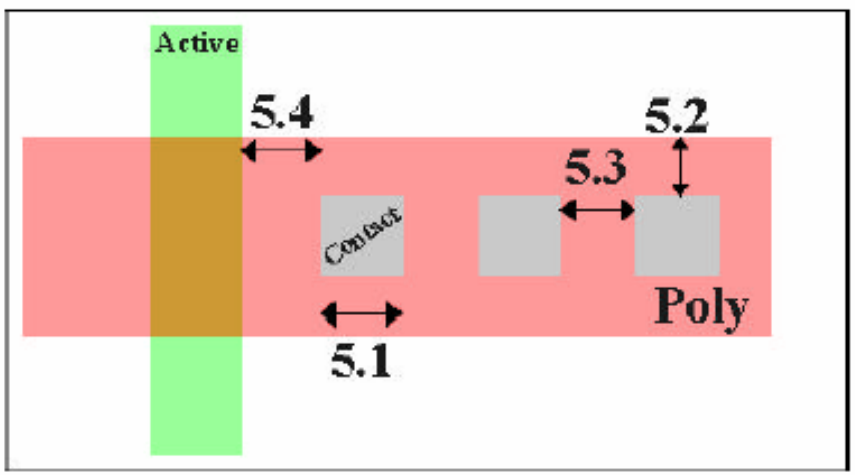
Rule	Description	Lambda		
		SCMOS	SUBM	DEEP
3.1	Minimum width	2	2	2
3.2	Minimum spacing over field	2	3	3
3.2.a	Minimum spacing over active	2	3	4
3.3	Minimum gate extension of active	2	2	2.5
3.4	Minimum active extension of poly	3	3	4
3.5	Minimum field poly to active	1	1	1

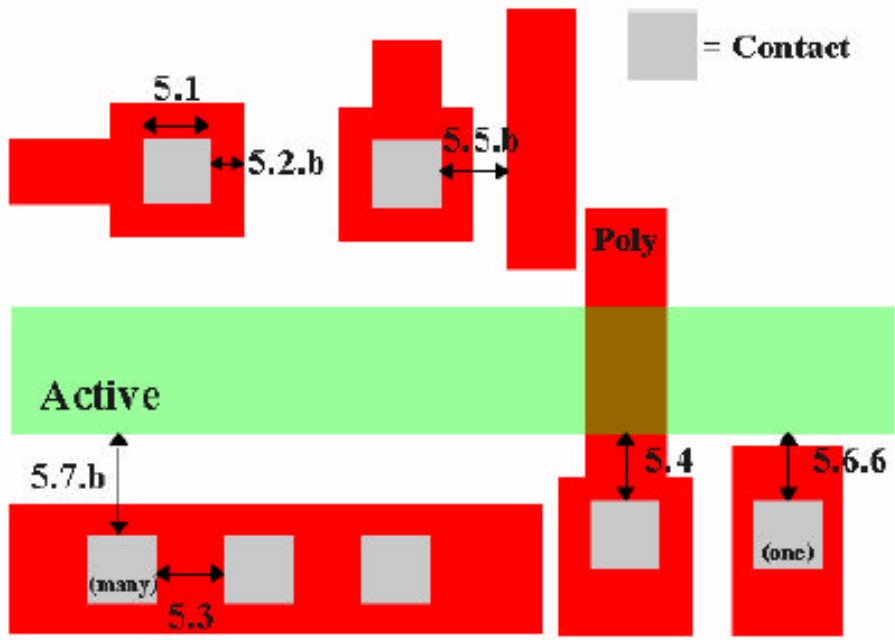


Contact to Poly

Rule	Description	Lambda		
		SCMOS	SUBM	DEEP
5.1	Exact contact size	2x2	2x2	2x2
5.2	Minimum poly overlap	1.5	1.5	1.5
5.3	Minimum contact spacing	2	3	4
5.4	Minimum spacing to gate of transistor	2	2	2

Rule	Description	Lambda		
		SCMOS	SUBM	DEEP
5.2.b	Minimum poly overlap	1	1	1
5.5.b	Minimum spacing to other poly	4	5	5
5.6.b	Minimum spacing to active (one contact)	2	2	2
5.7.b	Minimum spacing to active (many contacts)	3	3	3

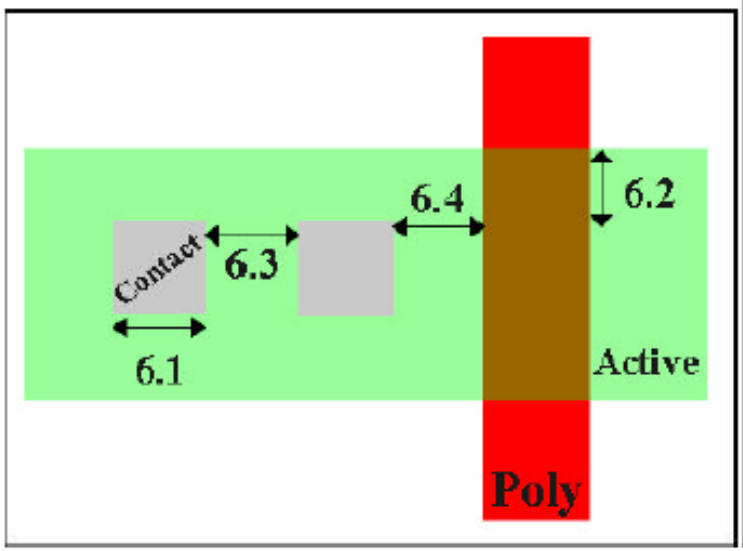


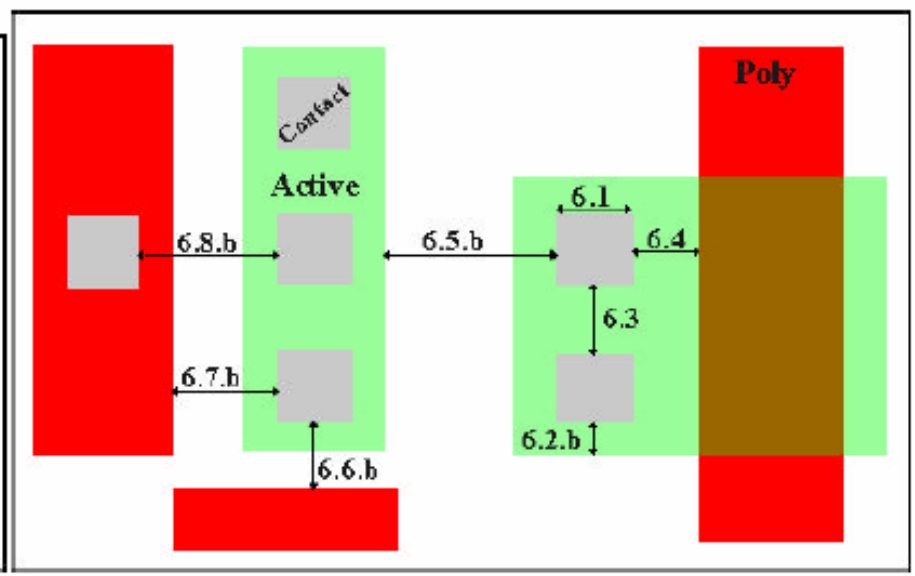


Contact to Active

Rule	Description	Lambda		
		SCMOS	SUBM	DEEP
6.1	Exact contact size	2x2	2x2	2x2
6.2	Minimum active overlap	1.5	1.5	1.5
6.3	Minimum contact spacing	2	3	4
6.4	Minimum spacing to gate of transistor	2	2	2

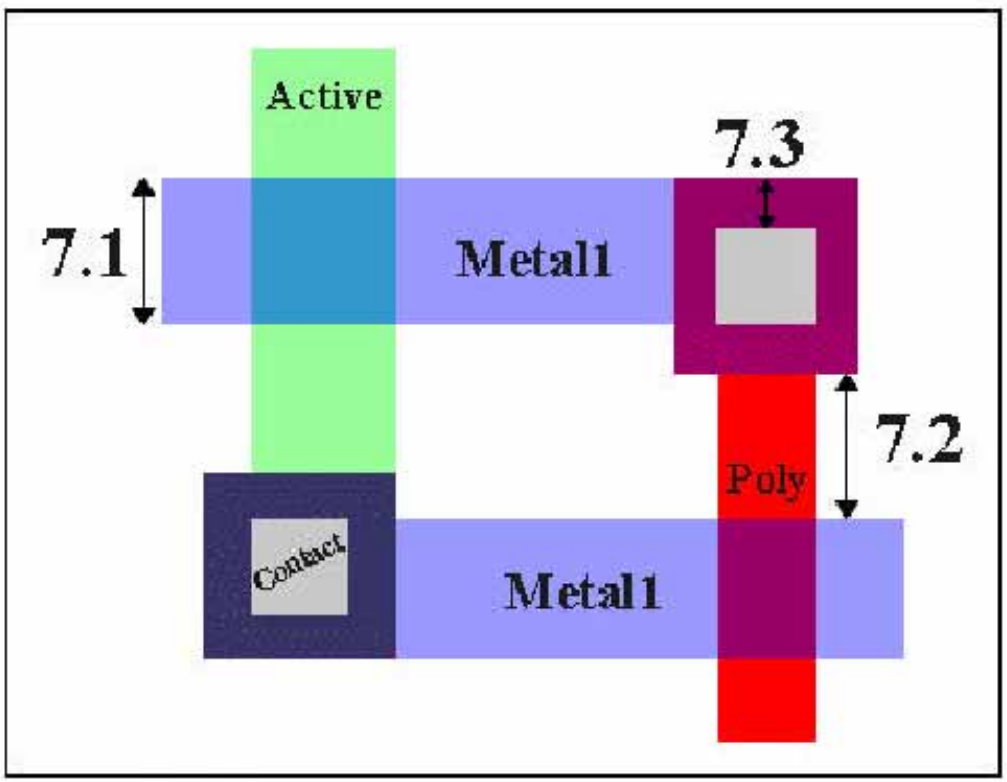
Rule	Description	Lambda		
		SCMOS	SUBM	DEEP
6.2.b	Minimum active overlap	1	1	1
6.5.b	Minimum spacing to diffusion active	5	5	5
6.6.b	Minimum spacing to field poly (one contact)	2	2	2
6.7.b	Minimum spacing to field poly (many contacts)	3	3	3
6.8.b	Minimum spacing to poly contact	4	4	4





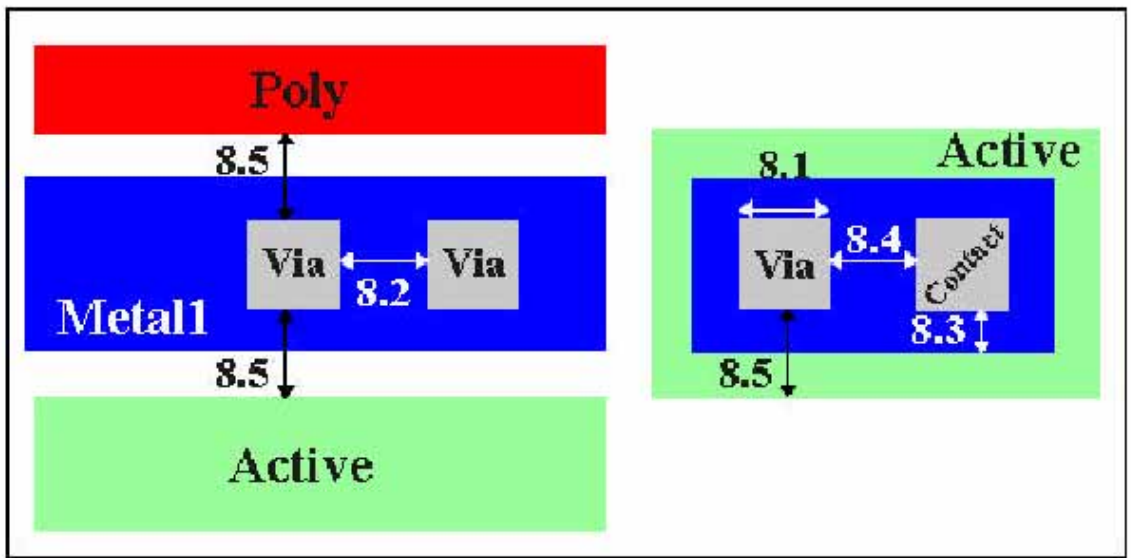
Metal 1

Rule	Description	Lambda		
		SCMOS	SUBM	DEEP
7.1	Minimum width	3	3	3
7.2	Minimum spacing	2	3	3
7.3	Minimum overlap of any contact	1	1	1
7.4	Minimum spacing when either metal line is wider than 10 lambda	4	6	6



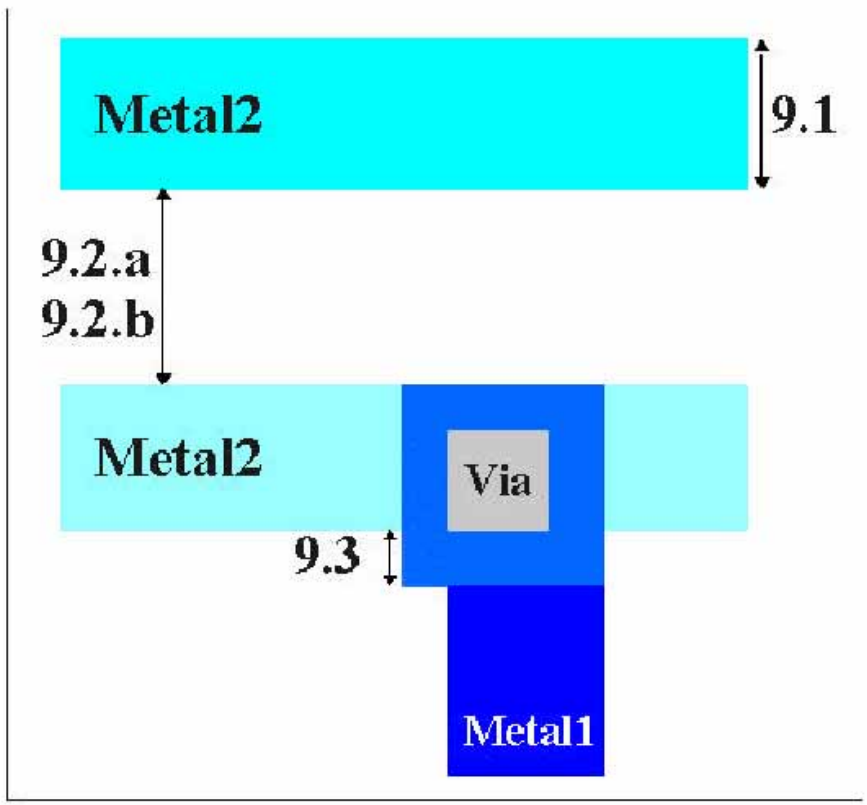
Via

Rule	Description	Lambda					
		2 Metal Process			3+ Metal Process		
		SCMOS	SUBM	DEEP	SCMOS	SUBM	DEEP
8.1	Exact size	2 x 2	n/a	n/a	2 x 2	2 x 2	3 x 3
8.2	Minimum via1 spacing	3	n/a	n/a	3	3	3
8.3	Minimum overlap by metal1	1	n/a	n/a	1	1	1
8.4	Minimum spacing to contact for technology codes mapped to processes that do not allow stacked vias (SCNA, SCNE, SCN3M, SCN3MLC)	2	n/a	n/a	2	2	n/a
8.5	Minimum spacing to poly or active edge	2	n/a	n/a	2	2	n/a



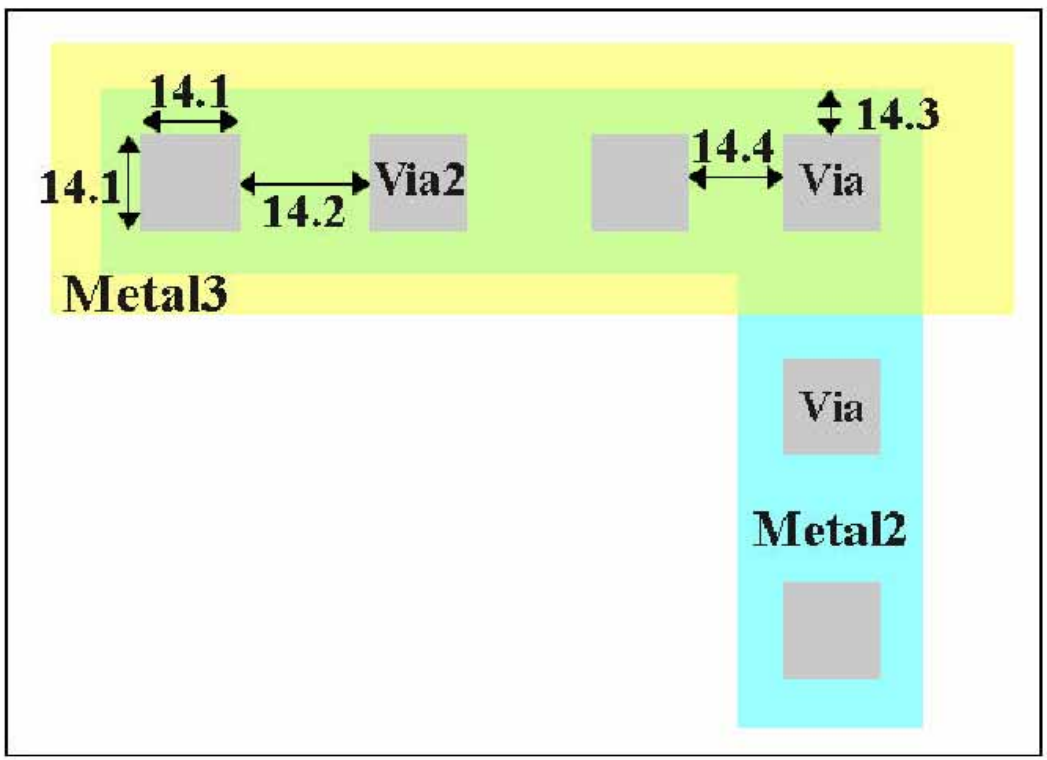
Metal 2

Rule	Description	Lambda					
		2 Metal Process			3+ Metal Process		
		SCMOS	SUBM	DEEP	SCMOS	SUBM	DEEP
9.1	Minimum width	3	n/a	n/a	3	3	3
9.2	Minimum spacing	3	n/a	n/a	3	3	4
9.3	Minimum overlap of via1	1	n/a	n/a	1	1	1
9.4	Minimum spacing when either metal line is wider than 10 lambda	6	n/a	n/a	6	6	8



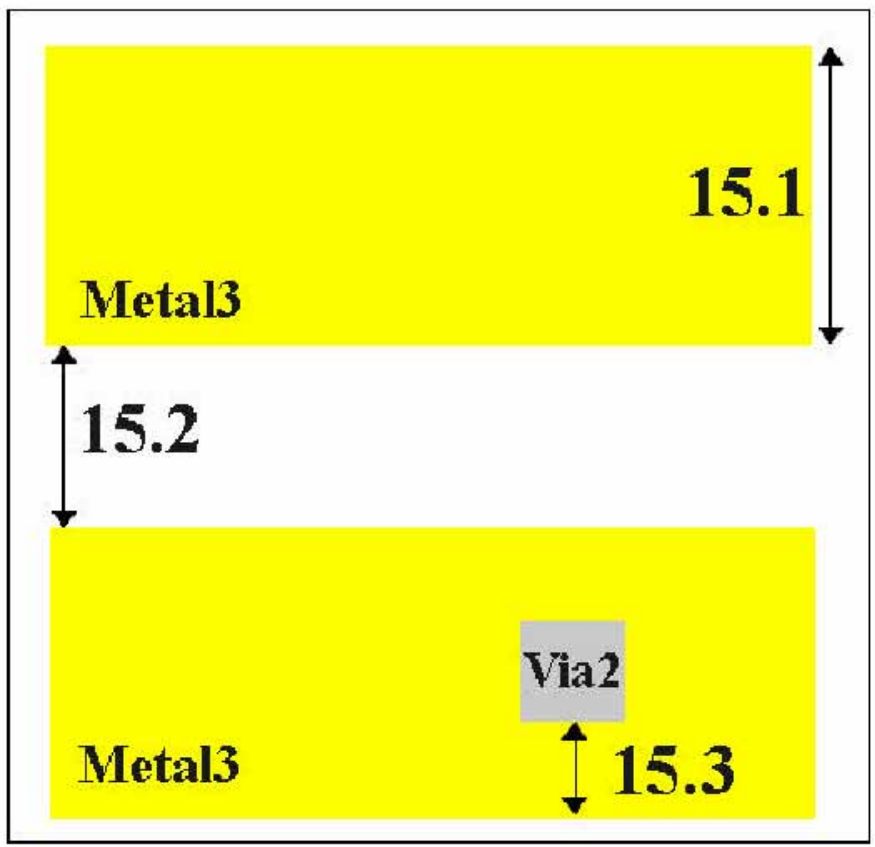
Via 2

Rule	Description	Lambda					
		3 Metal Process			4+ Metal Process		
		SCMOS	SUBM	DEEP	SCMOS	SUBM	DEEP
14.1	Exact size	2x2	2x2	n/a	2x2	2x2	3x3
14.2	Minimum spacing	3	3	n/a	3	3	3
14.3	Minimum overlap by metal2	1	1	n/a	1	1	1
14.4	Minimum spacing to via1 for technology codes that do not allow stacked vias (SCNA, SCNE, SCN3M, SCN3ME, SCN3MLC)	2	2	n/a	2	2	n/a
14.5	Via2 may be placed over contact						



Metal 3

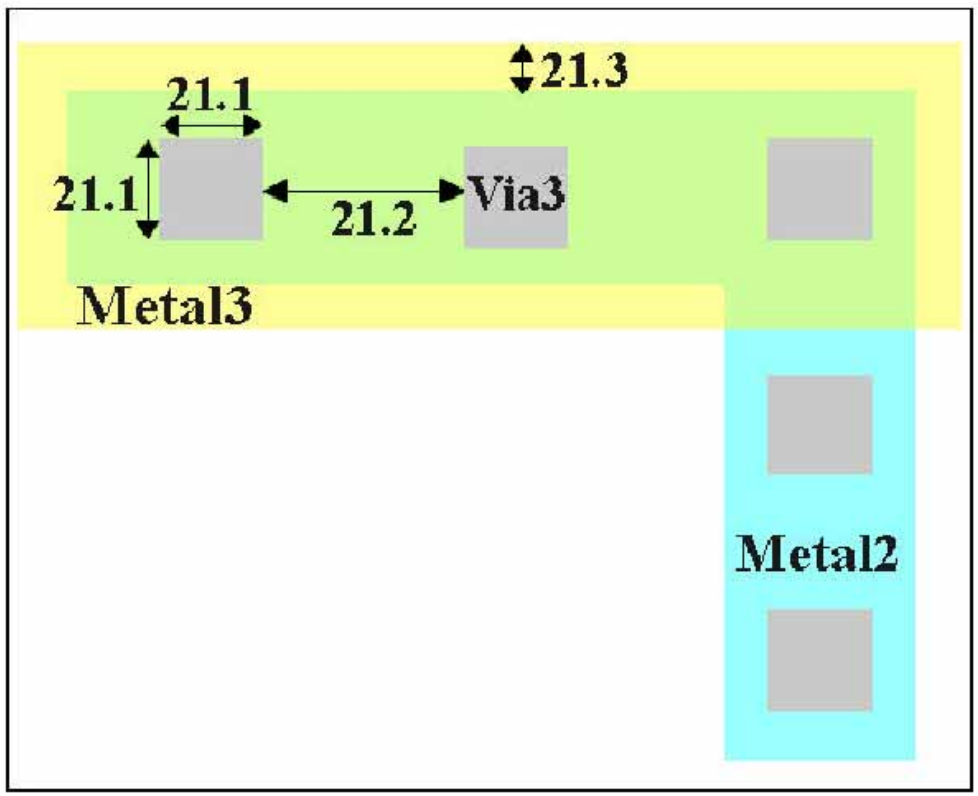
Rule	Description	Lambda					
		3 Metal Process			4+ Metal Process		
		SCMOS	SUBM	DEEP	SCMOS	SUBM	DEEP
15.1	Minimum width	6	5	n/a	3	3	3
15.2	Minimum spacing to metal3	4	3	n/a	3	3	4
15.3	Minimum overlap of via2	2	2	n/a	1	1	1
15.4	Minimum spacing when either metal line is wider than 10 lambda	8	6	n/a	6	6	8



Via 3

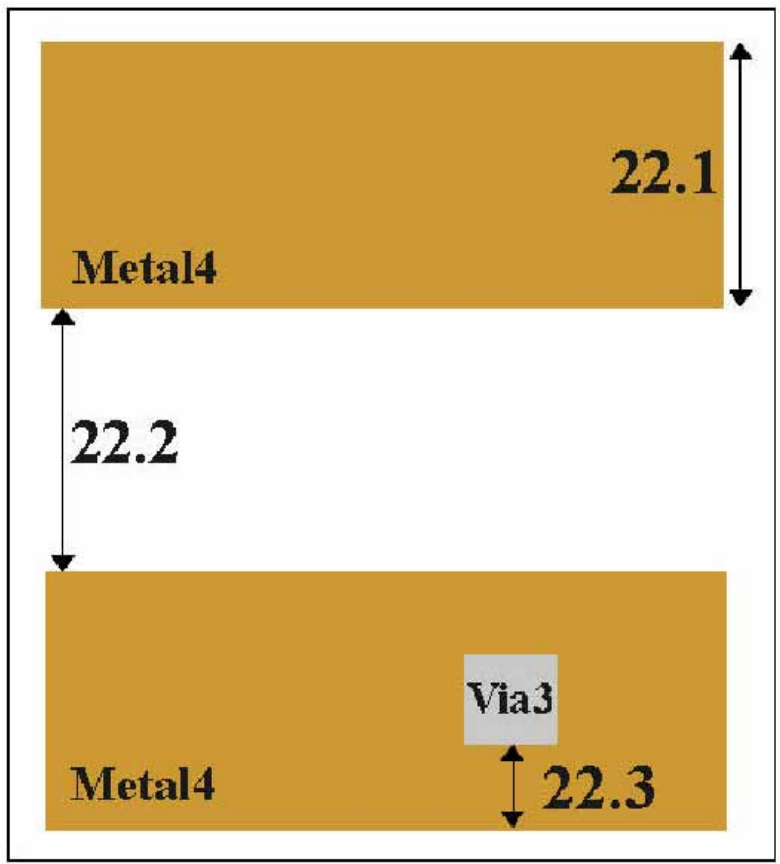
Rule	Description	Lambda					
		4 metal Process			5+ Metal Process		
		SCMOS	SUBM	DEEP	SCMOS	SUBM	DEEP
21.1	Exact size	2x2	2x2	n/a	n/a	2x2	3x3
21.2	Minimum spacing	3	3 *	n/a	n/a	3	3
21.3	Minimum overlap by Metal3	1	1	n/a	n/a	1	1

* Exception: Use lambda=4 for rule 21.2 only when using SCN4M_SUBM for Agilent/HP GMOS10QA 0.35 micron process



Metal 4

Rule	Description	Lambda					
		4 Metal Process			5+ Metal Process		
		SCMOS	SUBM	DEEP	SCMOS	SUBM	DEEP
22.1	METAL4 width	6	6	n/a	n/a	3	3
22.2	METAL4 space	6	6	n/a	n/a	3	4
22.3	METAL4 overlap of VIA3	2	2	n/a	n/a	1	1
22.4	Minimum spacing when either metal line is wider than 10 lambda	12	12	n/a	n/a	6	8



Via 4 and Metal 5

SCMOS Layout Rules - Via4
(SUBM and DEEP)

Vias must be drawn orthogonal to the grid of the layout. Non-Manhattan vias are not allowed.

Rule	Description	Lambda					
		5 Metal Process			6+ Metal Process		
		SCMOS	SUBM	DEEP	SCMOS	SUBM	DEEP
25.1	Exact size	n/a	2x2	3x3	n/a	2x2	3x3
25.2	Minimum spacing	n/a	3	3	n/a	3	3
25.3	Minimum overlap by Metal4	n/a	1	1	n/a	1	1

SCMOS Layout Rules - Metal5
(SUBM and DEEP)

Rule	Description	Lambda					
		5 Metal Process			6+ Metal Process		
		SCMOS	SUBM	DEEP	SCMOS	SUBM	DEEP
26.1	Minimum width	n/a	4	4	n/a	3	3
26.2	Minimum spacing to Metal5	n/a	4	4	n/a	3	4
26.3	Minimum overlap of Via4	n/a	1	2	n/a	1	1
26.4	Minimum spacing when either metal line is wider than 10 lambda	n/a	8	8	n/a	6	8

Via 5 and Metal 6

SCMOS Layout Rules - Via5 (SUBM and DEEP)

Vias must be drawn orthogonal to the grid of the layout. Non-Manhattan vias are not allowed.

Rule	Description	Lambda		
		6 Metal Process		
		SCMOS	SUBM	DEEP
29.1	Exact size	n/a	3 x 3	4 x 4
29.2	Minimum spacing	n/a	4	4
29.3	Minimum overlap by Metal5	n/a	1	1

SCMOS Layout Rules - Metal6 (SUBM and DEEP)

Rule	Description	Lambda		
		6 Metal Process		
		SCMOS	SUBM	DEEP
30.1	Minimum width	n/a	5	5
30.2	Minimum spacing to Metal6	n/a	5	5
30.3	Minimum overlap of Via5	n/a	1	2
30.4	Minimum spacing when either metal line is wider than 10 lambda	n/a	10	10

Summary of some important rules

Layer	Rules No.	Description	Lambda (deep submicron)
active	2.1	Minimum width	3
	2.2	Minimum spacing	3
poly	3.1	Minimum width	2
	3.2.a	Minimum spacing over active	4
	3.3	Minimum gate extension of active	2.5
	3.4	Minimum active extension of poly	4
contact	5.1	Exact size	2 x 2
	5.2 (5.2b, 7.3)	Minimum overlap	1.5 (1)
Metal 1	7.1	Minimum width	3
	7.2	Minimum spacing	3
Via 1, 2, 3, 4	8.1, 14.1, 21.1, 25.1	Exact size	3 x 3
	8.3, 14.3, 21.3, 25.3	Minimum overlap	1
Metal 2, 3, 4, 5	9.1, 15.1, 22.1, 26.1	Minimum width	3
	9.2, 15.2, 22.2, 26.2	Minimum spacing	4
Via 5	29.1	Exact size	4 x 4
	30.3	Minimum overlap	2
Metal 6	30.1	Minimum width	5
	30.2	Minimum spacing	5