Layout-Implementation

Layout Concept & Virtuoso

- Generic CMOS Process Flow
  - Deep sub-micron(feature size<0.25um) process
  - Process technology
- Basic Layout Concept
- Layout and Devices
- Layout Design Consideration
- Layout tool—Virtuoso
- I/O PAD

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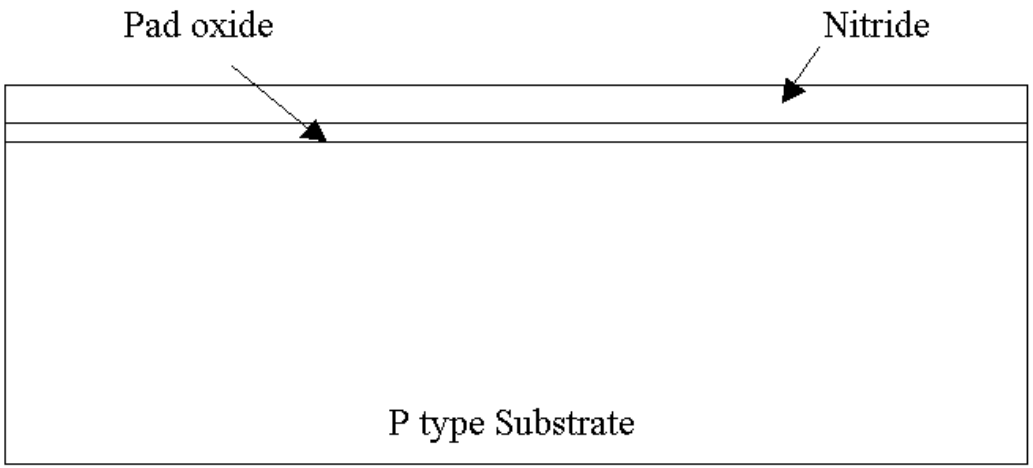
Deep sub-micron process

- The deep sub-micron generic CMOS process flow is described below.
- It features shallow trench isolation (STI), dual n+/p+ polysilicon gates, and self-aligned silicide.

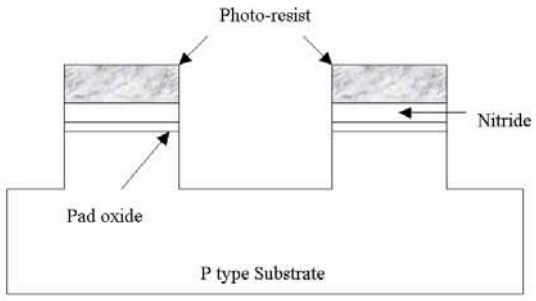
p-type substrate

- Starting material p-type substrate or p- epi on p+ substrate for latch-up prevention.
- Grow pad oxide. Deposit CVD nitride

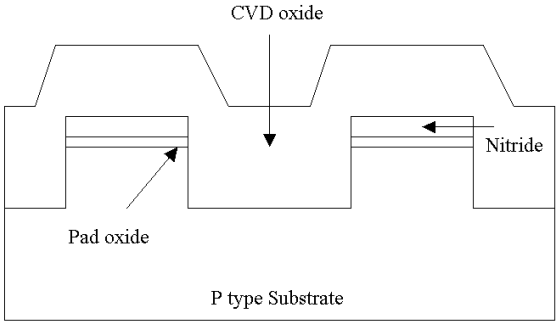


Shallow Trench Isolation

- Lithography to cover the active region with photoresist.
- Reactive ion etching(RIE) nitride and oxide in the field region.
- RIE shallow trench in silicon.

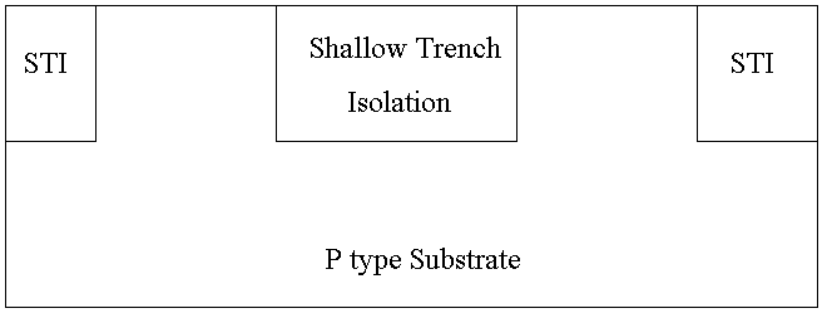


- Grow pad oxide. Deposit thick CVD oxide.

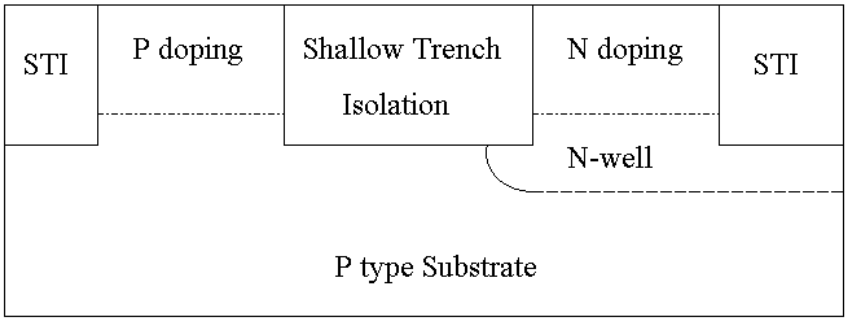


CMP & Implant

- Chemical-mechanical polishing (CMP) planarization

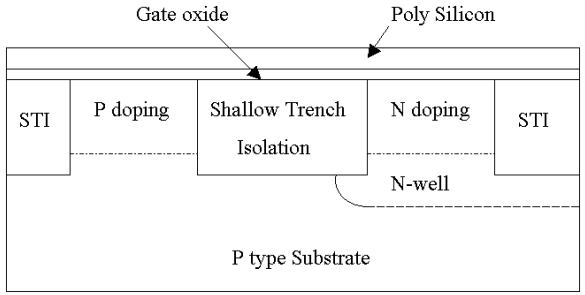


- p-well lithography and implant(also channel doping).

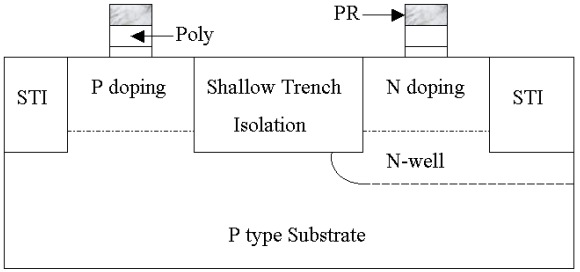


Making Poly

- Grow gate oxide.
- Deposit polysilicon film.

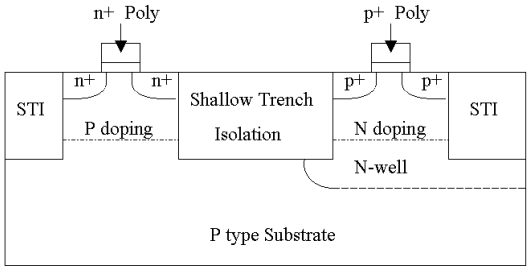


- Gate lithography.
- RIE polysilicon gate.

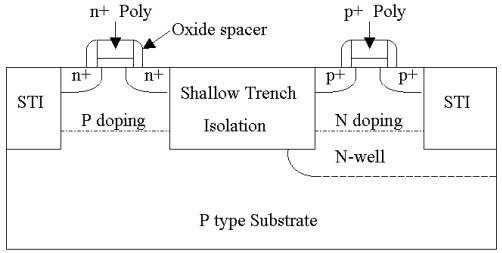


Source-Drain Implant

- Sidewall reoxidation.
- n+ source-drain lithography and implant (also dope n+ polysilicon gate).
- p+ source-drain lithography and implant (also dope p+ polysilicon gate).

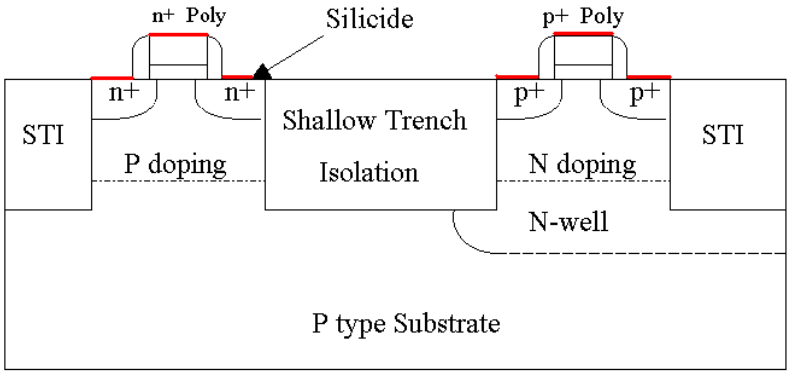


- Oxide (or nitride) spacer formation by CVD and RIE.
- Source-drain anneal.



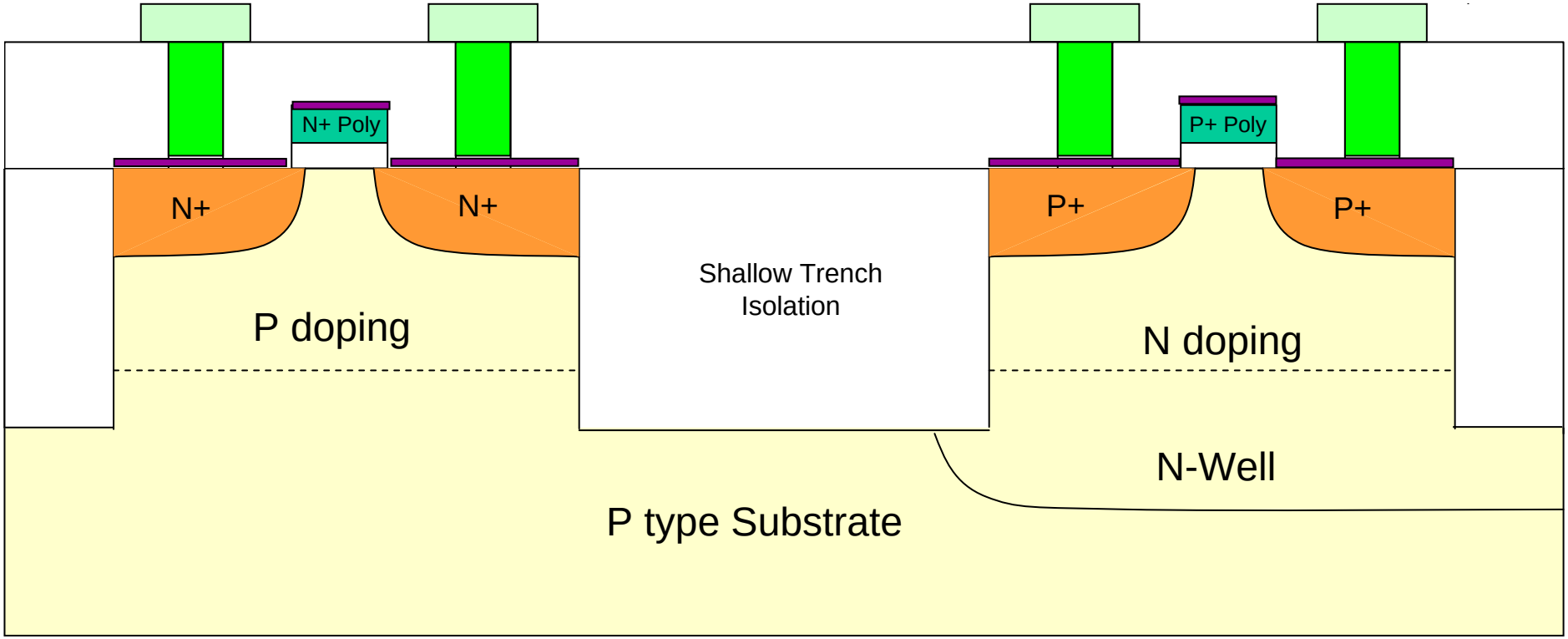
Silicide

- Self-aligned silicide process.



- Back-end-of-the-line process.

Generic CMOS process flow



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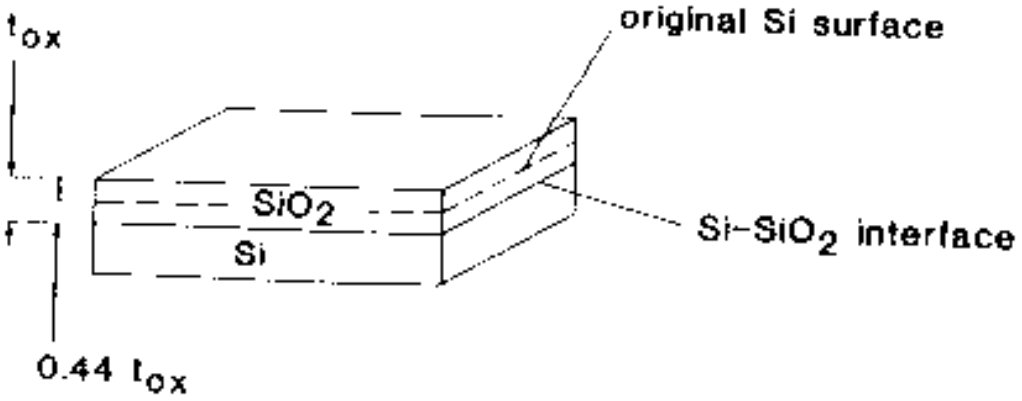
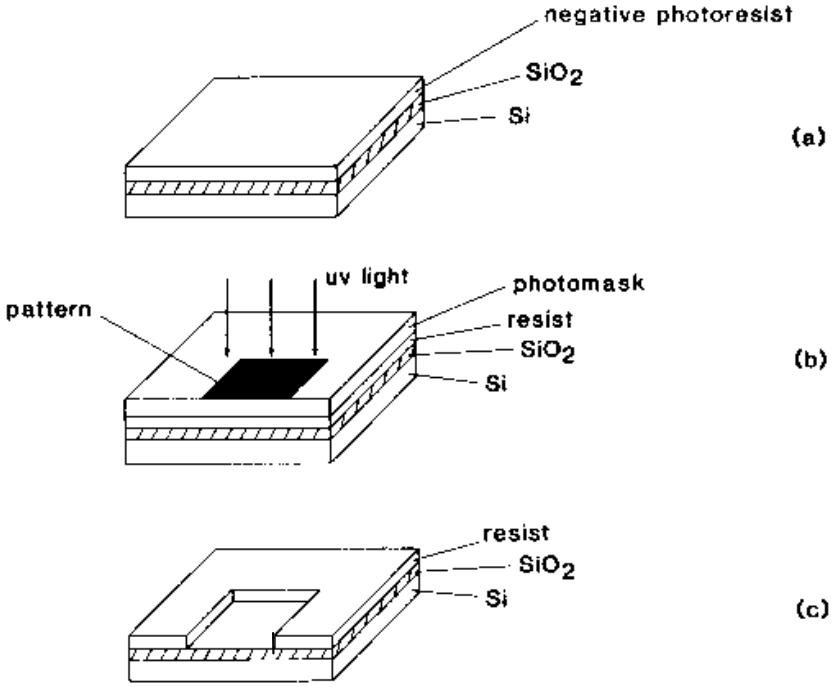
Oxidation

- A protective layer of *SiO2* is grown over the silicon surface by exposing the surface to oxygen (dry oxidation) or steam (wet oxidation) in a furnance at 800~1200℃.
- Dry oxidation is denser/slower than wet oxidation
- The resulting *Si-SiO2* interface will be below the original *Si* surface. For an oxide thickness *tox*, the shift is 0.44 *tox*.



Photolithography (photomasking)

- Establish patterns for the selective deposition or removal of material such as *SiO2*.
- contact printing : the mask is in close physical contact with the wafer. (good resolution/damage to the mask surface)
- projection printing : allowing a small gap (10 ~30um) between the wafer and the mask.



Etching

- **Wet etching** : unprotected *SiO2* can be removed by immersing the wafer in *HF*.
- **Dry etching** (plasma-assisted etching) : a partial ionized gas (plasma) is used to remove the unprotected *SiO2* for the wafer. (more accuracy than the wet one).The remaining photoresist can be removed by solvant or a plasma process.

Diffusion(Introduce dopants into silicon)

- **Performed by two step:**

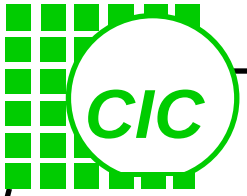
1) **Predeposition** : a specified density of dopant atoms is introduced into the silicon surface by exposing the silicon surface to a carrier gas at a high temperature.
2) **Drive-in** : impurities penetrate into the material deeper by heating the wafer.

Deposition

- ***SiO2***, ***Si3N4***, and ***aluminum*** can be deposited to form a thin film on wafers.
- **CVD (Chemical vapor deposition)** : a material is reacted at high temperature, and is deposited by way of a carier gas(*H2*/*N2*). This procedure can be used to deposit ***polysilicon***, ***SiO2***, and ***Si3N4***.
- **Vacuum evaporation** : the metal source and the wafer are placed in a vacuum chamber, the source is heated or bombarded by an electron beam to cause some of the matal atoms to leave the source.
- **Sputtering** : positive ions are generated in a gas discharge, and are accelerated by a high voltage to a cathode which is coated by the source metal.

Ion implantation (introduce impurities into silicon)

- Ionized atoms of the dopant are extracted from a gas and separated using magnetic deflection.
- The ions are then accelerated by a high voltage (50~150keV) and the resulting ion beam focus on the wafer surface.
- The penetration depth of the dopant atoms is typically around 1um.
- The impact of the ion beam causes some damage to the single-crystal silicon structure, a annealing step is usually needed.



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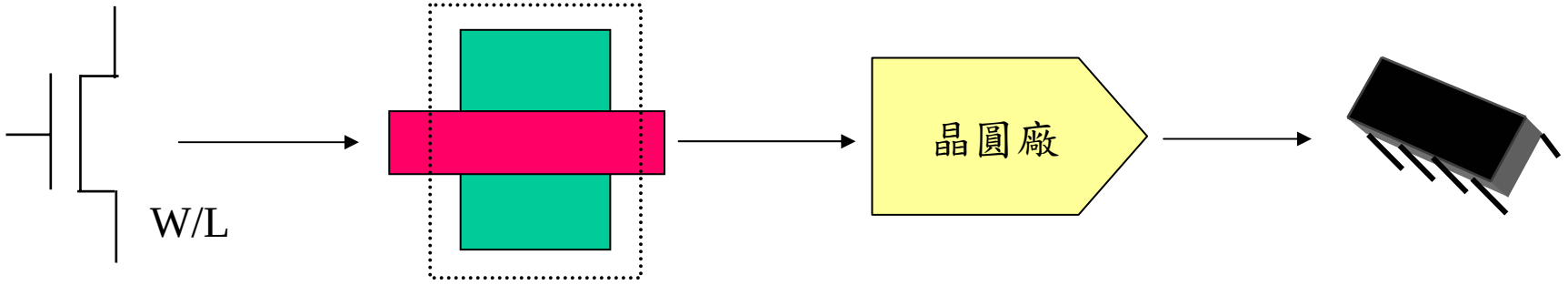
Basic Layout Concept

- 電路設計及模擬的驗證決定電路的組成及元件相關參數，但仍不是實體的成品
- 積體電路的實際成品需經晶圓廠製作。
- 設計者需提供積體電路製作的實體描述,即佈局
- 佈局設計將所設計的電路轉換為電路製作的描述格式
- 階層化、模組化的佈局方式可提高佈局的效率
- Layout Editor 或 P&R 工具提供佈局設計的環境



Layout Manual

- Brief process flow
- Masking layers and bias
- Layout design rule(RF design rule)
- Design guideline(RF design guideline)
- Electrical design rule
- Characterization reports-describe the characteristic of devices

製程技術資料

於選定製程並完成電路設計後，需取得相關技術資料以利佈局之進行，佈局資料主要包含：

- Design Rule
  - 佈局規則，可靠度設計參考規範
- 設計環境設定檔
  - 使用層次及顏色特性定義、佈局驗證命令檔

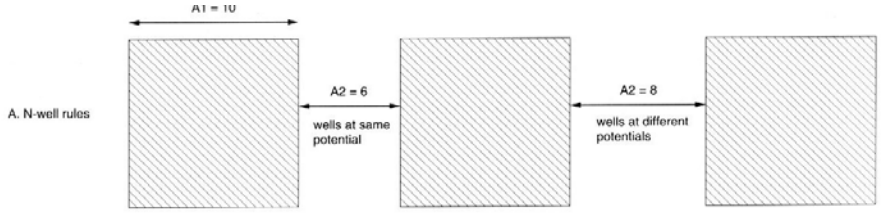
Mask Layer Definitions

Masking Sequence	Definition	Digitized Pattern	Digitized Area
Diffusion	Define active region	Diffusion	D
T-Well	Define T-Well implant region	T-Well	C
N-Well	Define N-Well implant region	N-Well	C
P-Well	Define P-Well implant region	N-Well	D
Poly	Define Poly gate	Poly	D
HR	Define high resistance Poly region	HR	C
N+	Define N+ implant region	(*1)	C
P+	Define P+ implant region	P+	C
SAB	Define salicide block region	SAB	D
Contact	Define Poly and Diffusion Contact	Contact	C
Metal1	Define 1st Metal	Metal1	D
Mvia1	Define 1st and 2nd Metal Contacts	Mvia1	C
	⋮		
MMC	Define Metal/Metal Capacitor Top metal Plate	MMC	D
Mvia5	Define 5th and 6th Metal Contacts	Mvia5	C
Metal6	Define 6th Metal(*) or Top Metal	Metal6	D
Pad	Window Define Pad Window region	PAD Window	C
PESD	Define PESD implant region	PESD	C

Layout design rule(1)

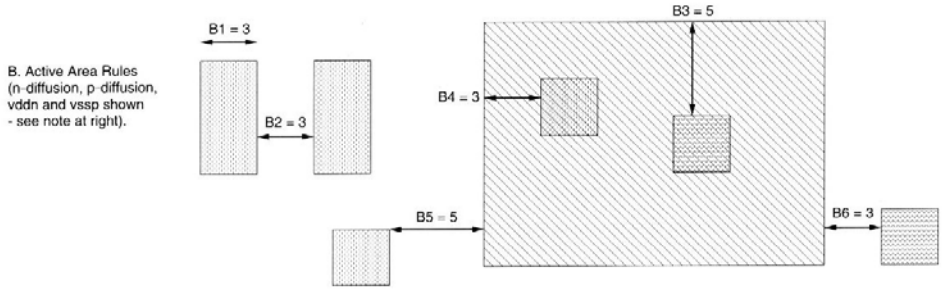
A.N-well layer

A.1 Minimum size	2u
A.2 Minimum spacing (well at same potential)	2u
A.3 Minimum spacing (well at different potential)	2u



B.Thin(Active) Area

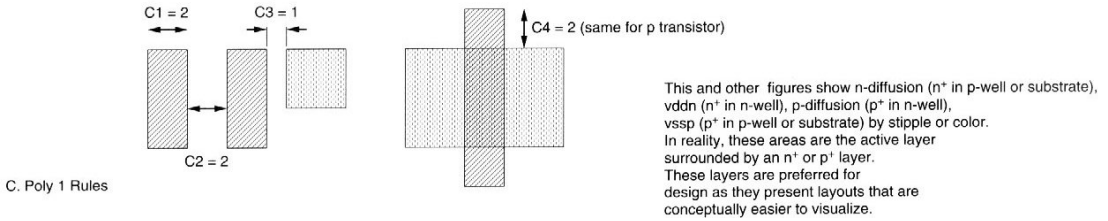
B.1 Minimum size	1u
B.2 Minimum spacing	1u
B.3 N-well overlap of p+	1u
B.4 N-well overlap of n+	1u
B.5 N-well space to n+	5u
B.6 N-well space to p+	3u



Layout design rule(2)

C.Poly 1

C.1 Minimum size	1u
C.2 Minimum spacing	1u
C.3 Spacing to Active 0.5u	
C.4 Gate Extension	1u



C. Poly 1 Rules

- **Min. feature density rule** : Sub-micron fabrication processes often use CMP to achieve planarity. Effective CMP requires a minimum feature density for polysilicon and metal layers. Dummy metal(poly) pattern and empty areas should be distributed as uniformly as possible.

(e.g.) Minimum density(total metal2 layout area/chip area) of Metal2 area ------ 30%

- **Antenna rule** : prevent the potential damages induced by the charge collected in the fabrication process on exposed polysilicon and metal features connected to a transistor. The accumulated charge may develop potentials sufficiently high to damage the thin oxide.

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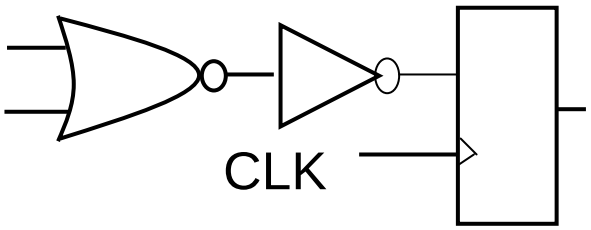
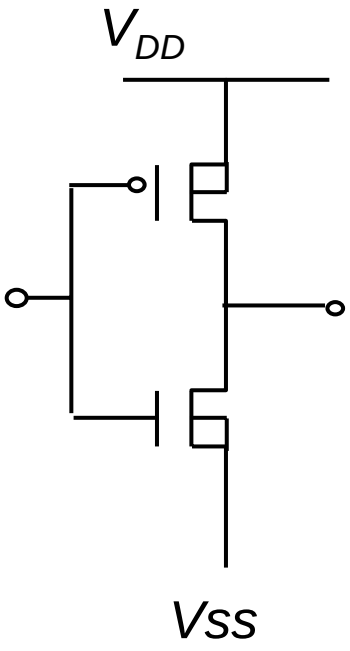
Design Abstraction

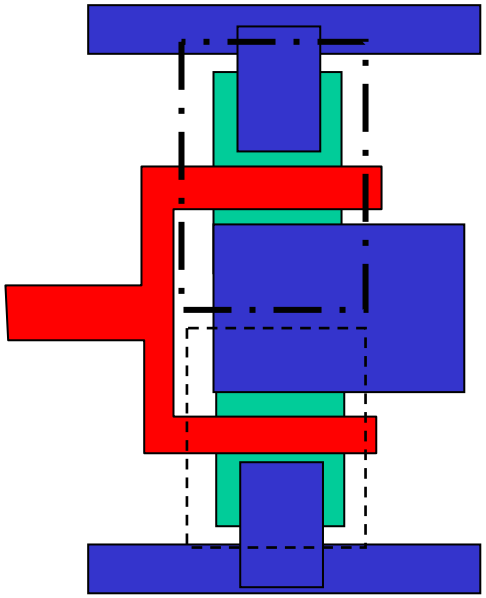
Gate and Connect
- Functionality
- Complexity



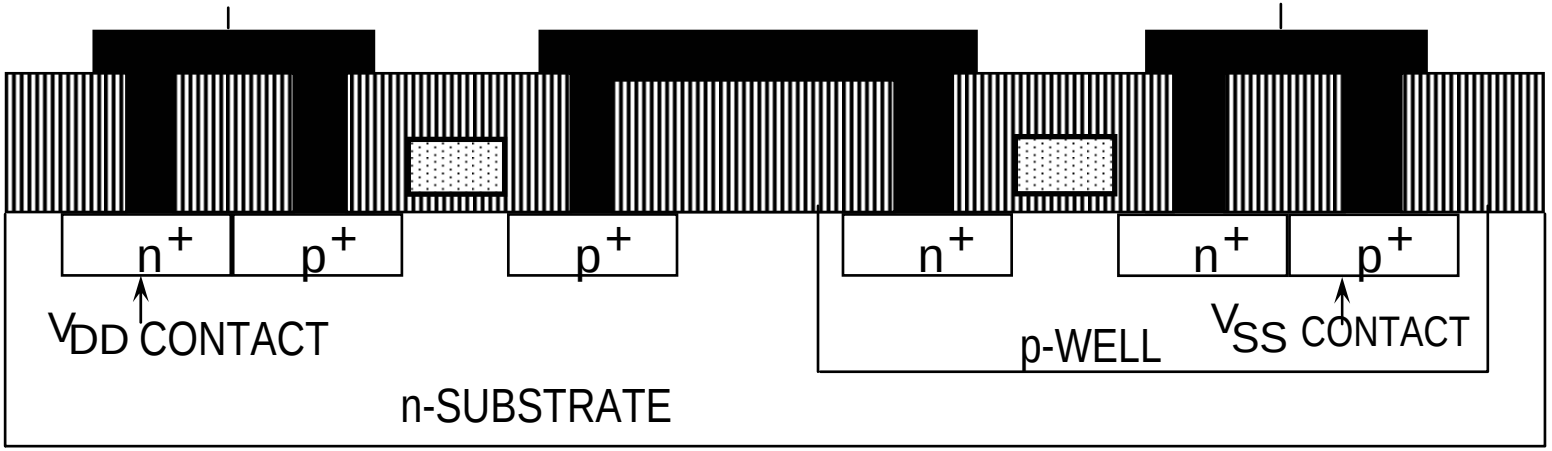
Device and Interconnect
- Performance
- Characteristic

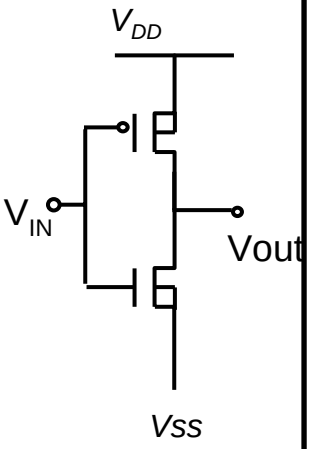


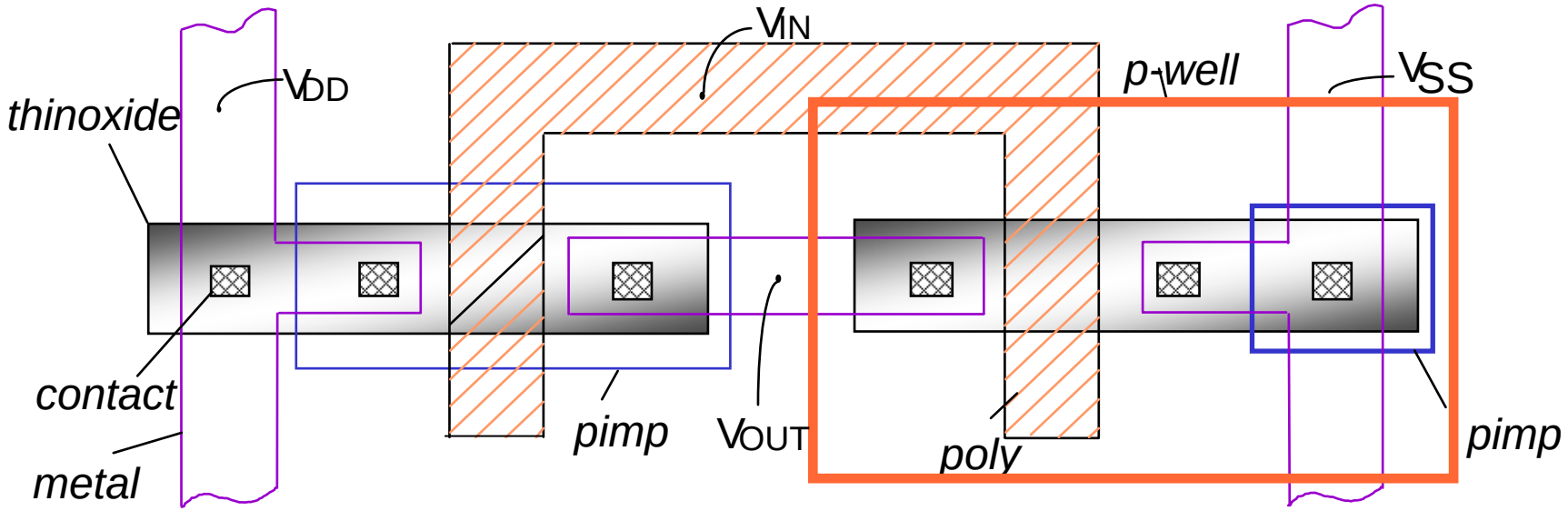
Geometry Object
- Fabrication
- Area/Cost
- Performance



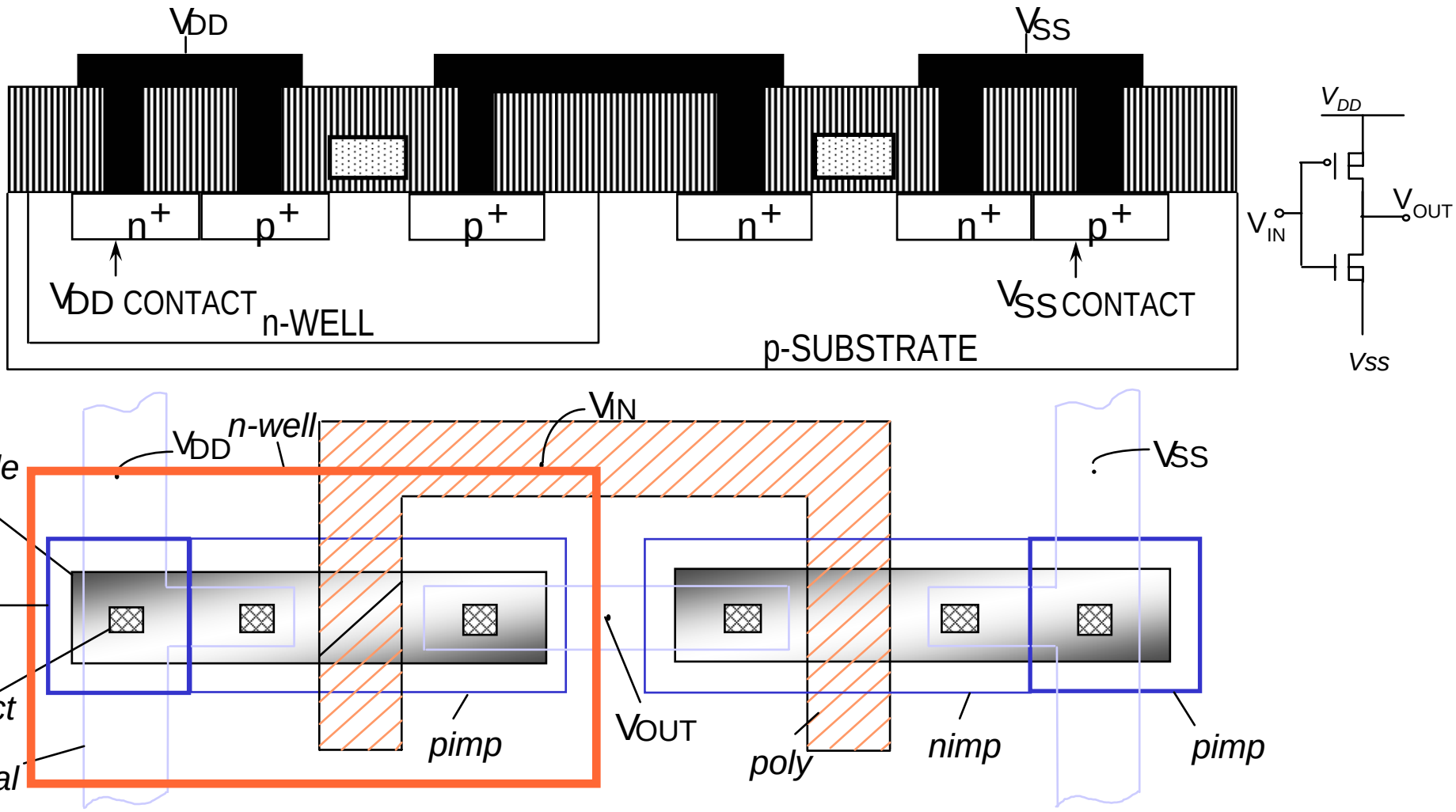
電晶體結構圖(Pwell製程)





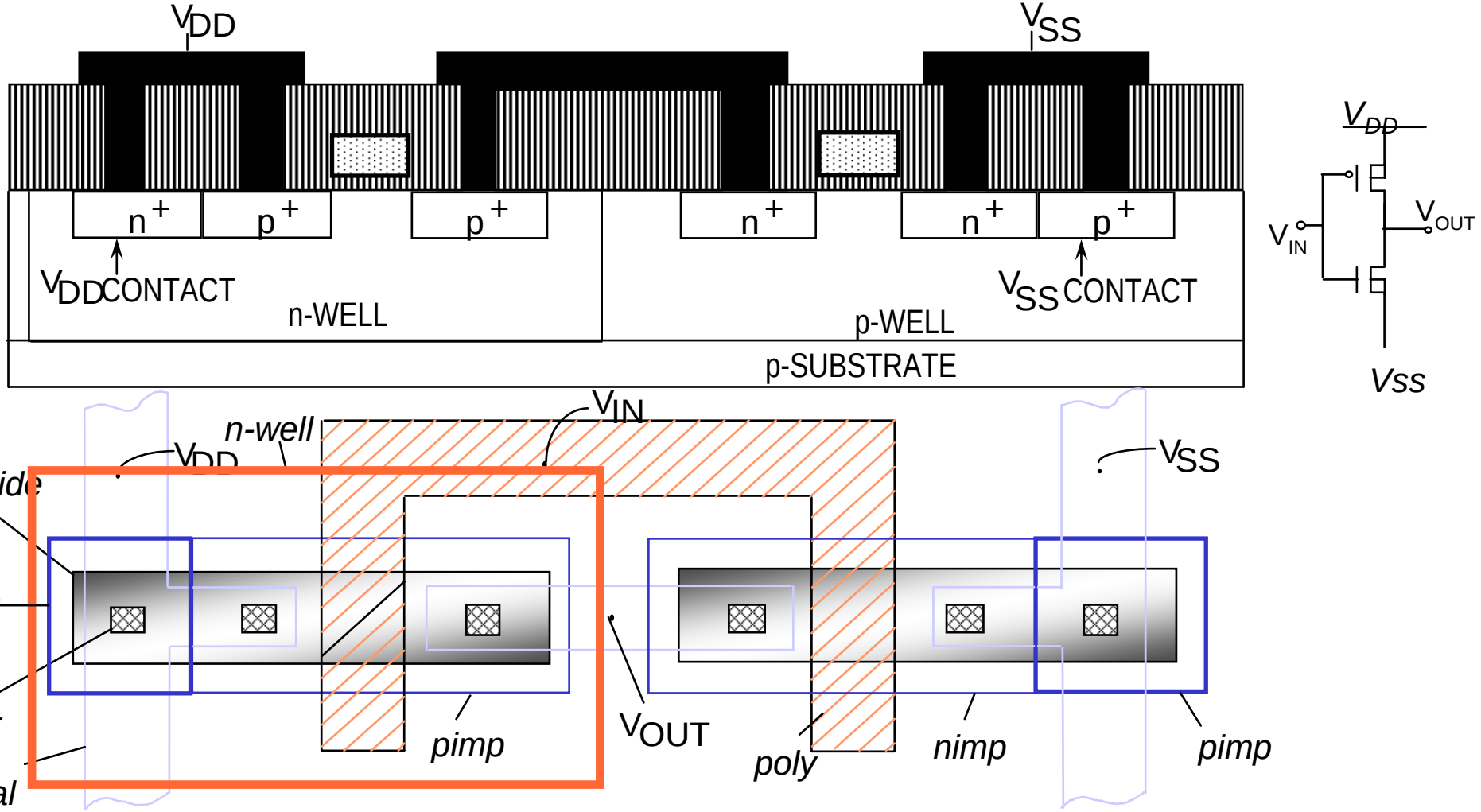


電晶體結構圖(Nwell製程)



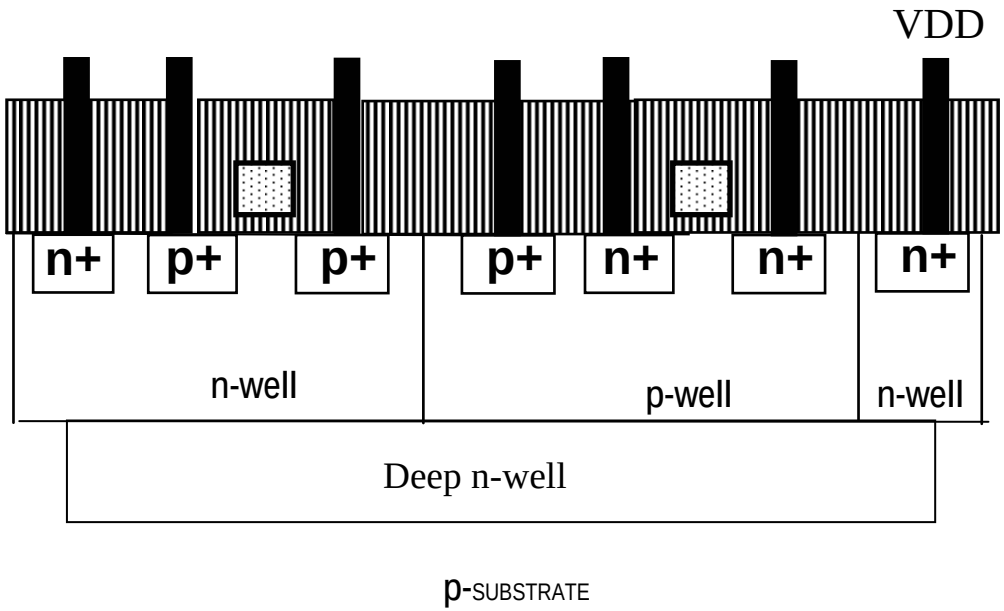
The cross-section view and layout of a CMOS(n-well) inverter

電晶體結構圖(Twinwell製程)



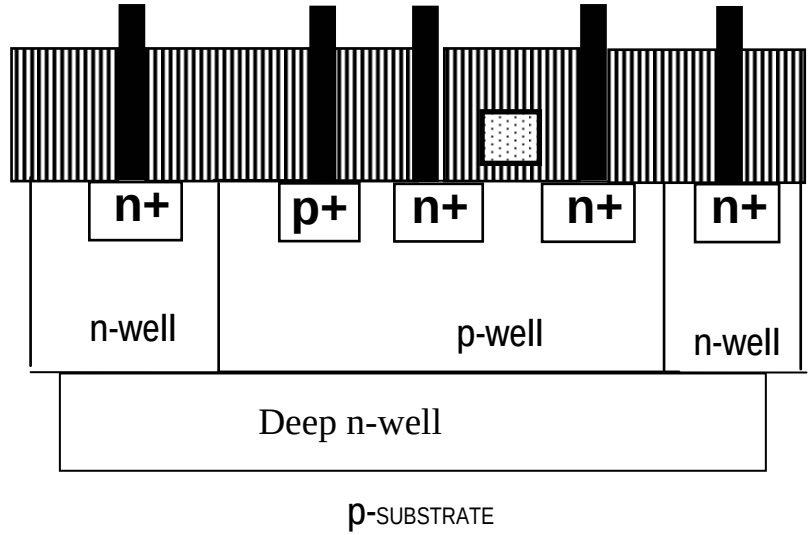
The cross-section view and layout of a CMOS(twin-well) inverter
(for 0.5um, 0.35um process of CIC)

PMOS(of core) in Deep Nwell (triple well process)

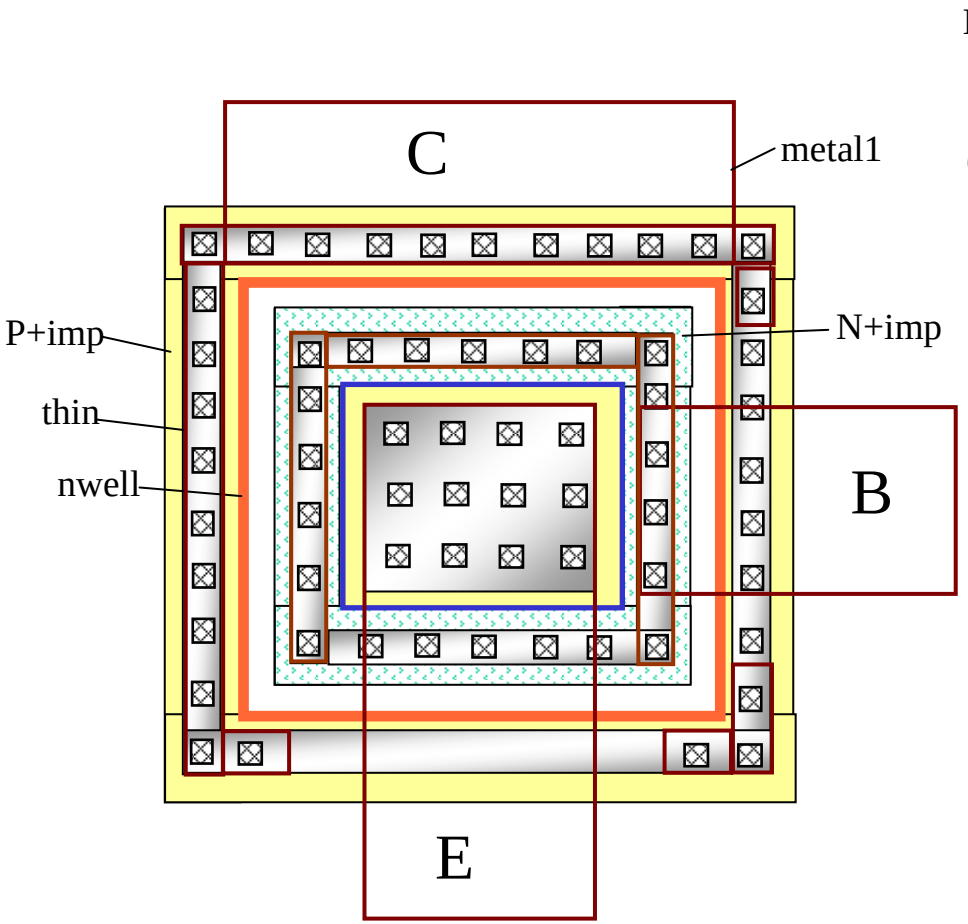


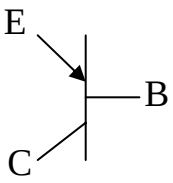
The bias of deep n-well should be a “clean” DC bias if this deep n-well is used as a shield.

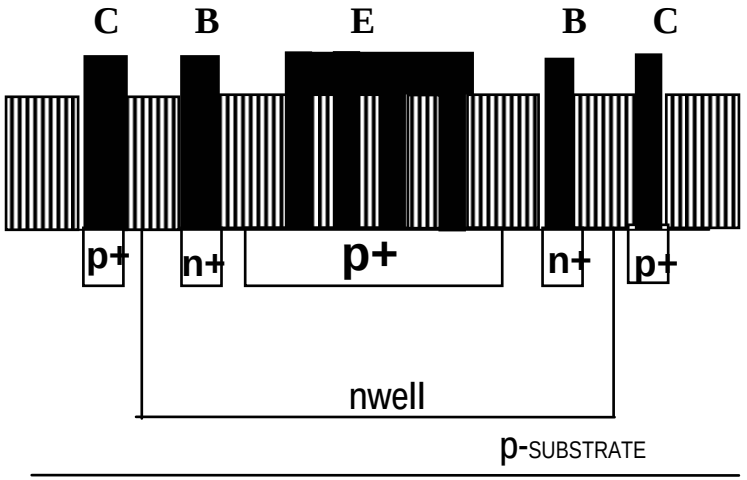
NMOS in Deep Nwell(triple well process)



Vertical P+/NW/Psub (PNP)

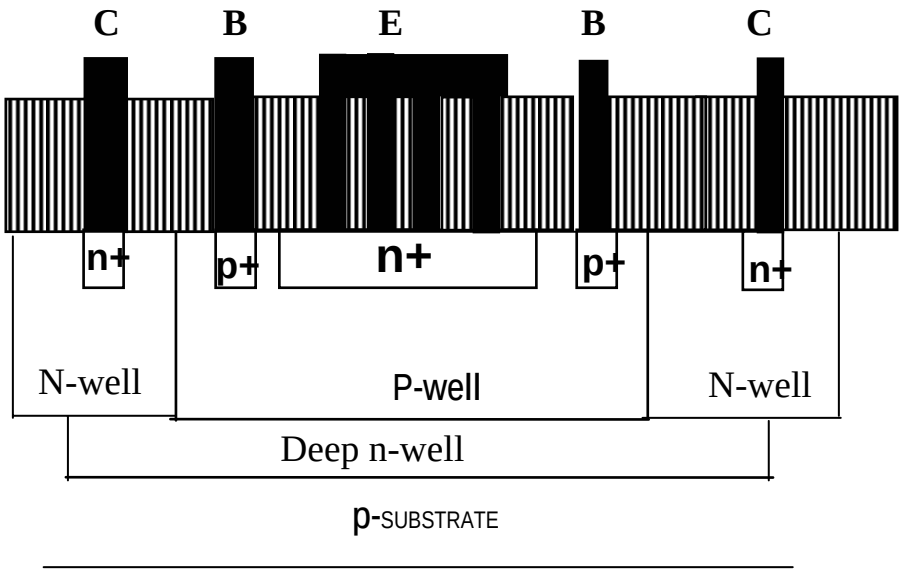






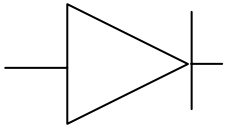
Vertical N+/Pwell/DNW(E/B/C) NPN

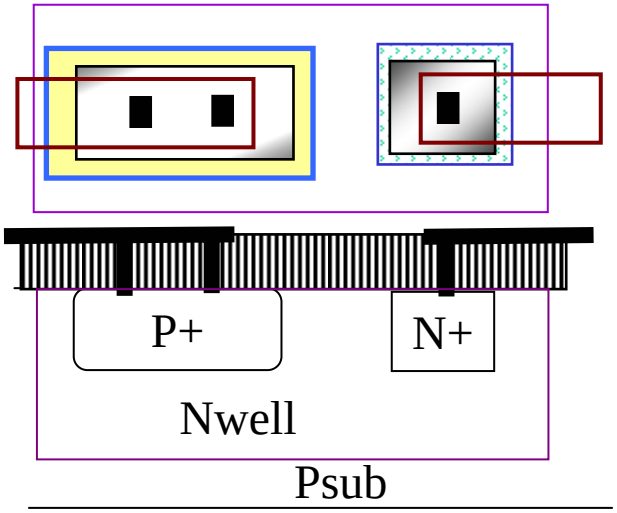
(triple well process)



CMOS製程中的二極體

A. P+/NW

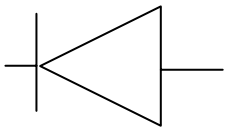


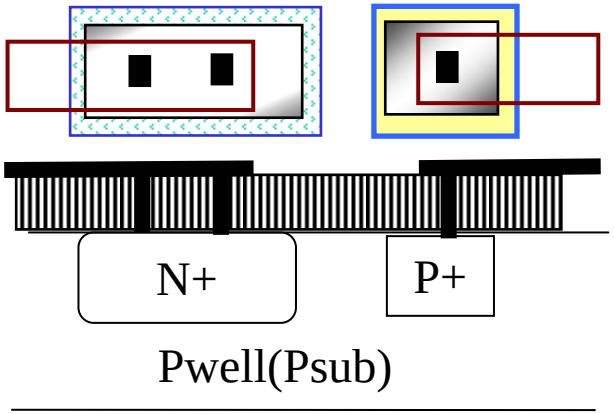


在CMOS製程中，二極體係利用P-N接面來實現，使用上必需確保其他接面都是逆向偏壓。

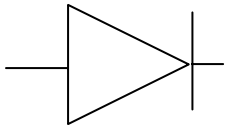
CMOS製程中的二極體

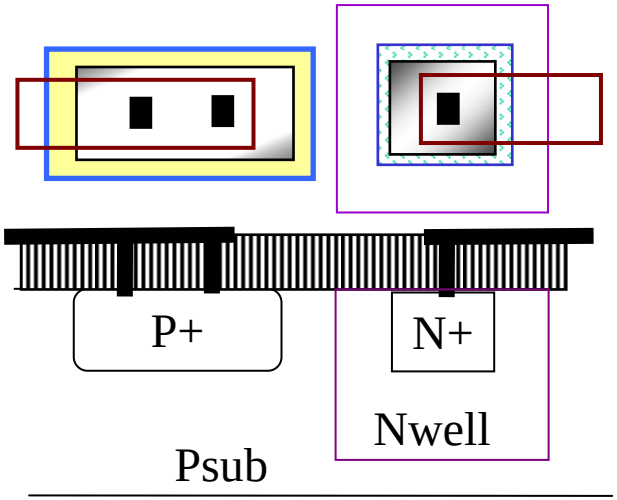
B. N+/PW





C. NW/Psub



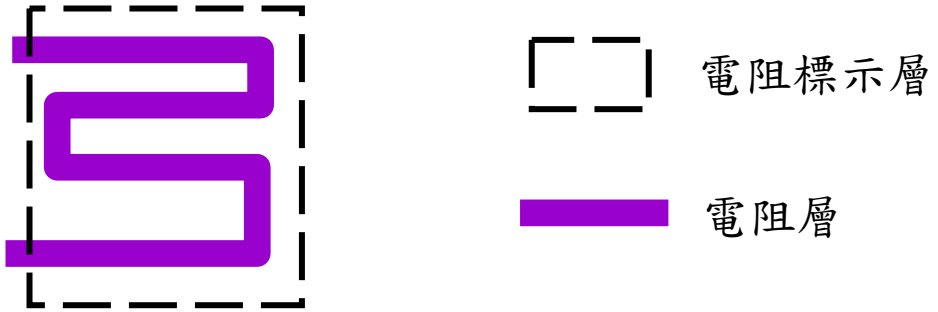


Resistor(1)

✓IC製程中若無特定步驟來製作電阻，可使用一般的導電層來製作電阻
✓電阻的實現須參考製程資料之單位方塊電阻值來設計, 並參考其對製成之變異度

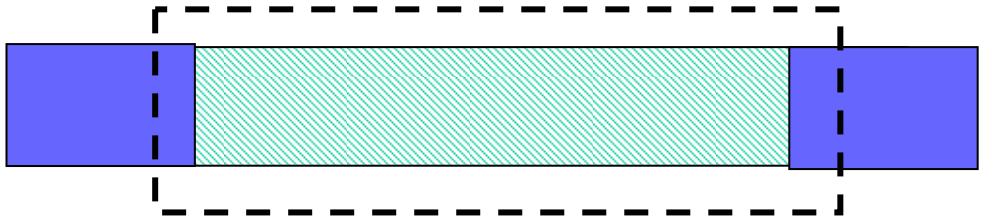
單位電阻值 :
Well > Diffusion(w/o silicide) > Poly (w/i silicide) > metal

電阻值的計算： $R_{\square} * L / W$
其中 單位電阻值$R_{\square}$: Ω/□



Resistor(2)

Poly, Diffusion 電阻(電阻標示層的畫法需和command file 配合)



Select poly cut Resis polyR

電阻標示層

電阻值：Rs * L/W = Rs * L/(Area/ Length)

注意：Silicide製程 之 Diffusion 電阻需加SAB (Salicide-Block) layer以避免因Silicide的製作造成低電阻值

Well 電阻

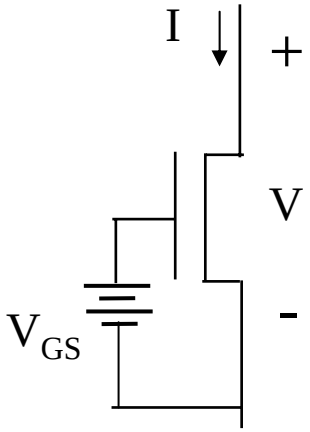
N-imp + THIN

Resistor(3)

電阻應用考量：

- 無法製作特定阻值的精密電阻
- 小的電阻值會有較大的誤差值
- 面積和電阻誤差值的取捨
- 使用電阻標示層(e.g.extR)供佈局驗證時萃取電阻
- 考量Contact 電阻值及 Bending 的電阻值

Active Resistor(1)



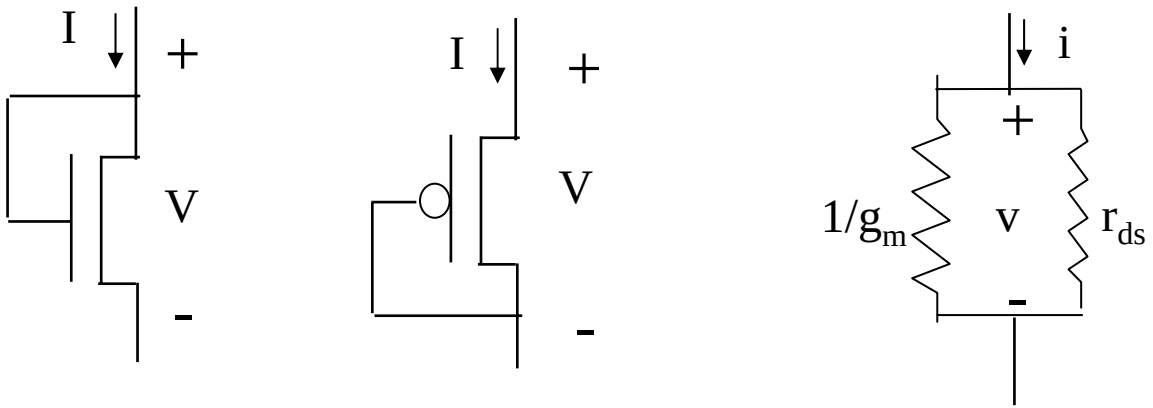
$R \approx 1/[K(V_{GS}-V_{t)}]$

$K = uC_{ox}W/L$

$V_{DS} < V_{GS}-V_t$

•Nonlinear resistor, operation in triode region

Active Resistor(2)



$$I=(K/2)(V-V_t)^2$$

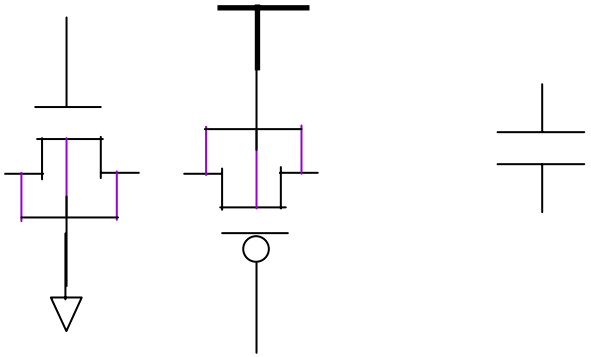
- Nonlinear resistor, can be used to produce a dc voltage drop and/or provide a small signal resistance that is linear over a small range.

Capacitor(1)

MOS製程的電容:

A. MOS Junction Capacitor

- nonlinear Capacitor
- 面積效益較高(C/area)
- Junctions remain reverse biased
- VGS > Vt (MOS linear region)



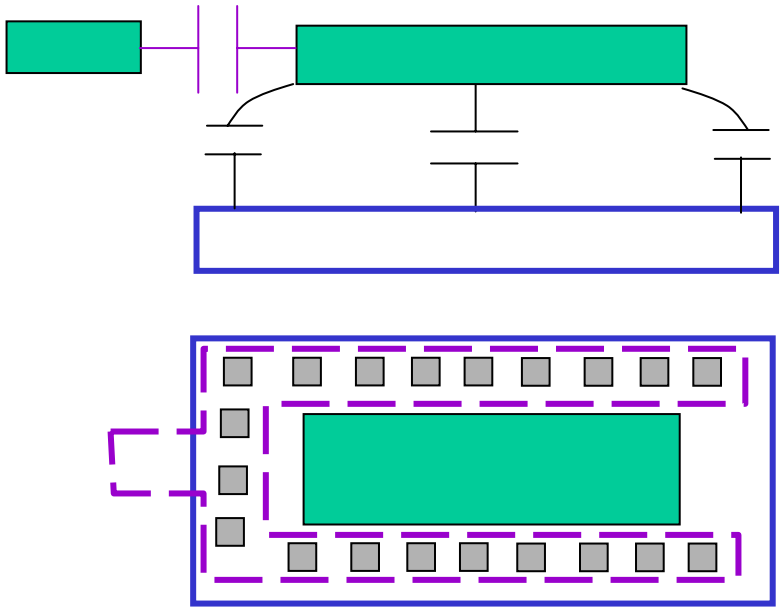
Capacitor(2)

B. Plate Capacitor

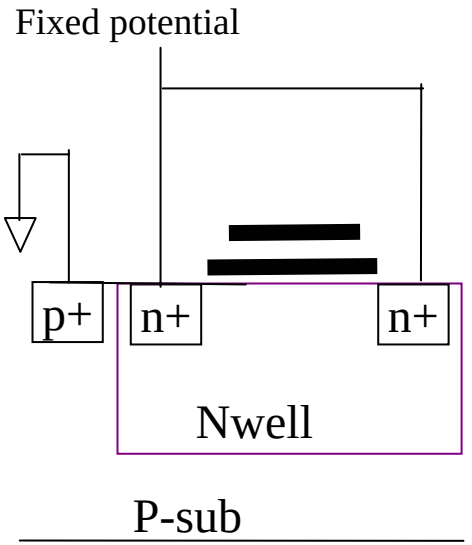
- 電容值較固定
- 構造簡單
- 電容值包含 Overlap Cap + Fringing Cap
- 額外光罩層可增加面積效益
  - Double poly 製程
  - MiM（Metal-insulator-Metal)製程

    (Metal Capacitor- 1fF/um2, Rs-top=0.4Ω/□, Rs-bottom=0.08 Ω /□)
    (Poly Capacitor- 1fF/um2, Rs-top=5 Ω /□, Rs-bottom=60 Ω /□)

Capacitor(3)



Poly-Poly Cap.



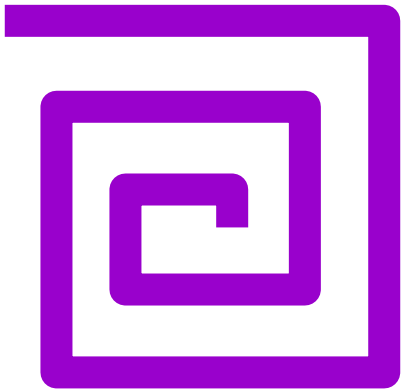
Use metals and wells as shield(is connected to fixed potential) to protect sensitive nodes

Inductor

在通訊應用中，電感可增加電路設計的效益，但在MOS製程中電感並非可良好控制之元件。

一般利用片電阻值較小之連接層(top_metal)來設計CMOS螺旋電感(spiral inductor)，但其主要問題為：

1. 電感值小
2. Q值小
3. 元件模型未充分建立，現階段需自行建立等效模型, RLC model

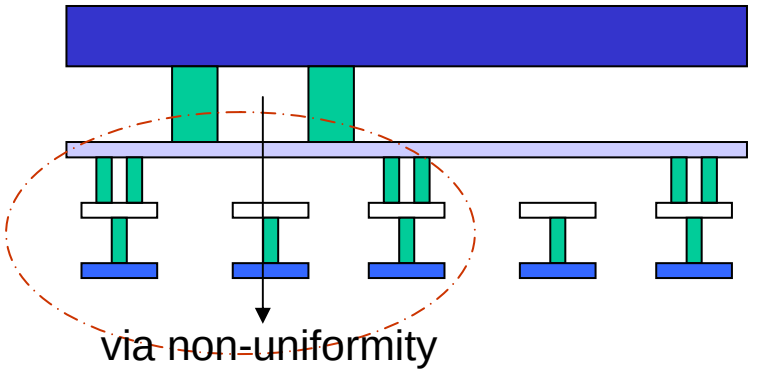


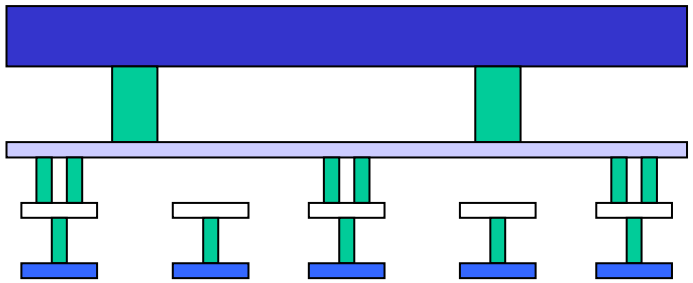
主動電感(active inductor)之問題:

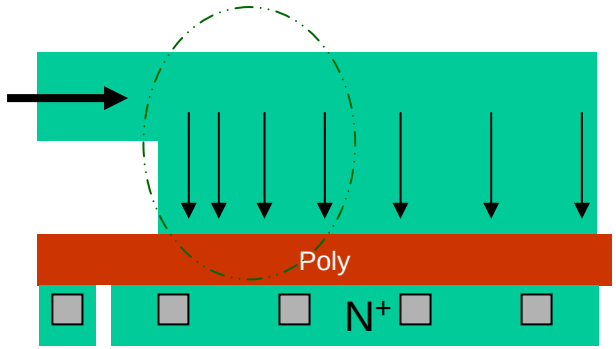
1.Induce higher noise
2.Distortion
3.Power consumption

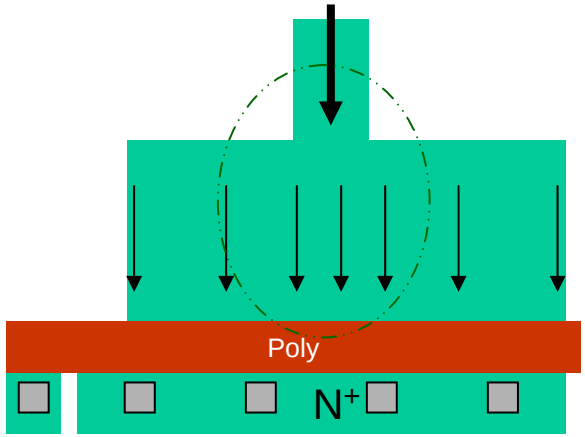
Bondwire Inductor
•typical values: 1nH/mm

Connection and Current Flow

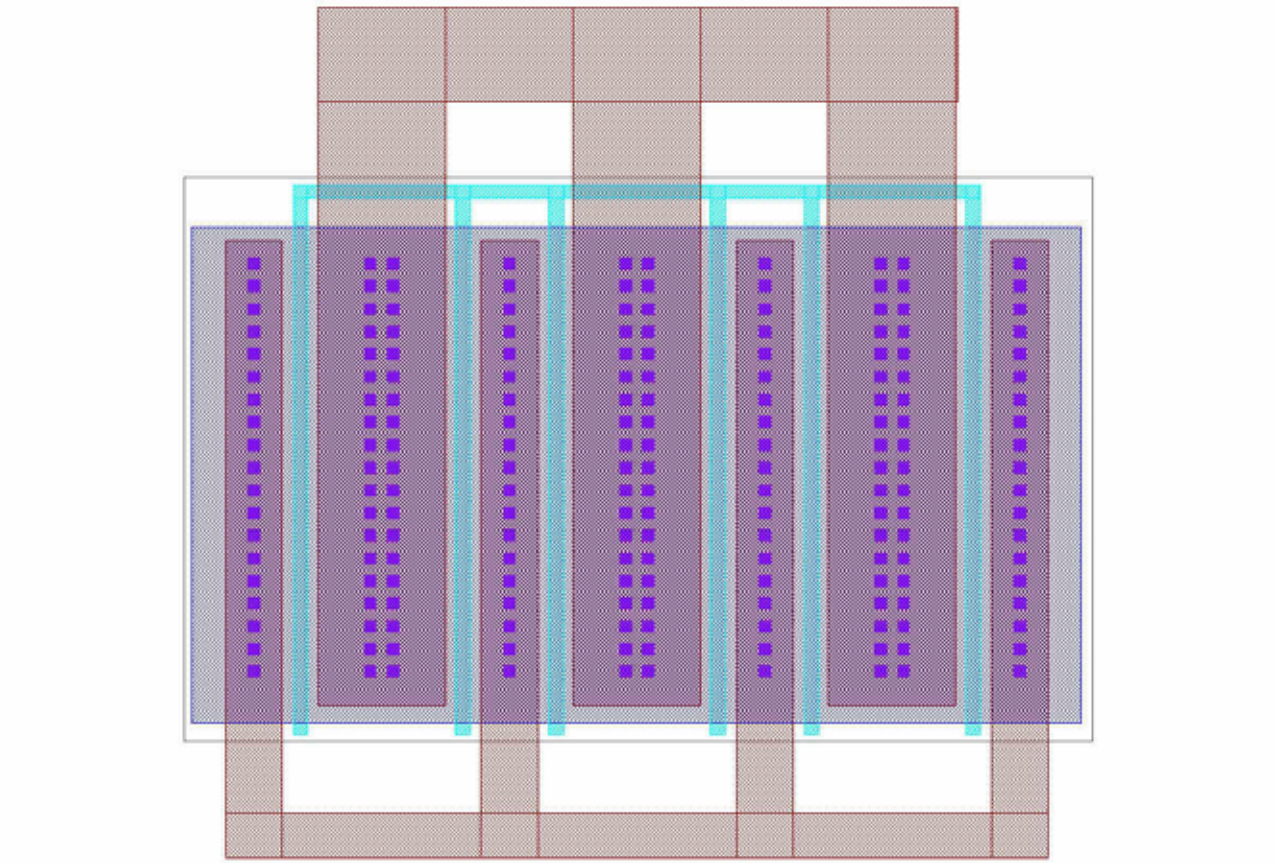




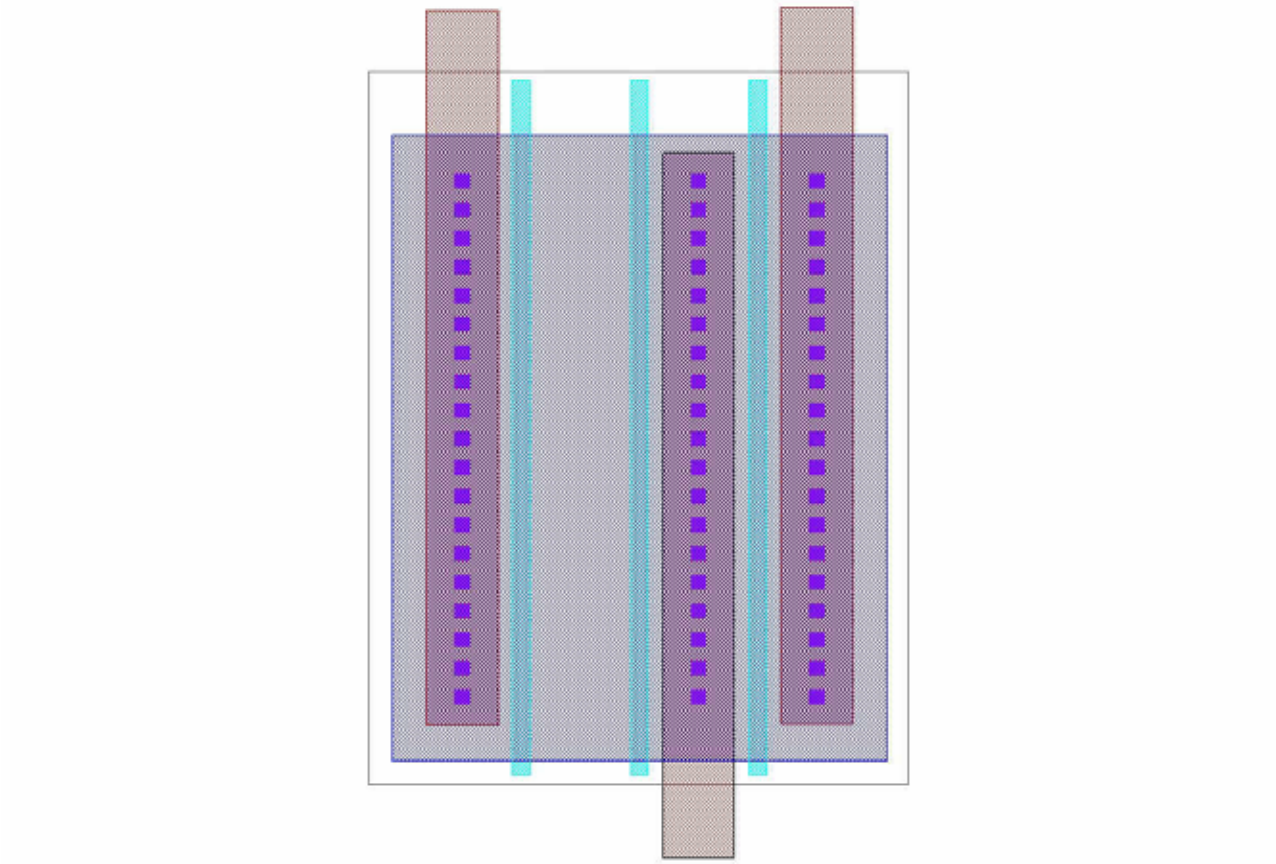




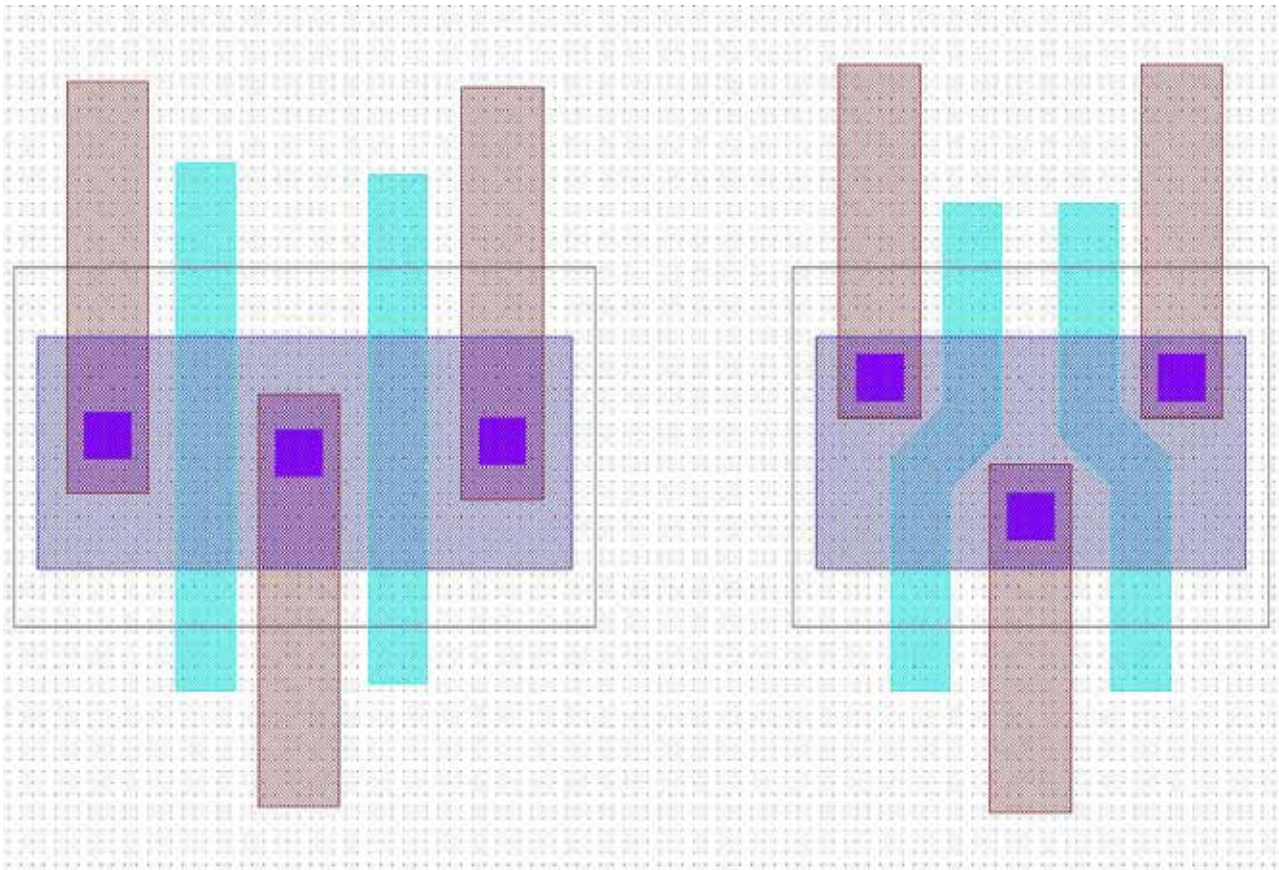
Multi - fingers



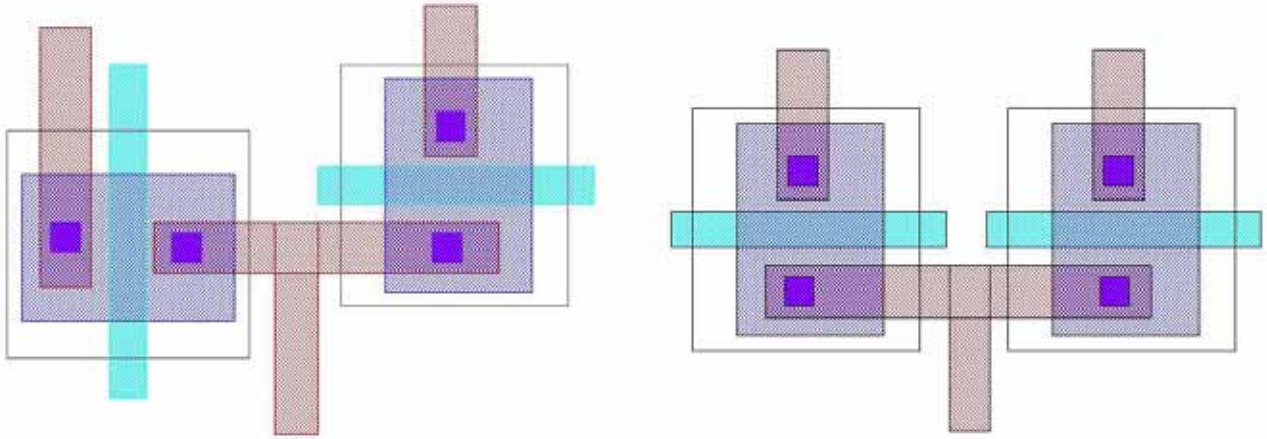
Sharing s/d



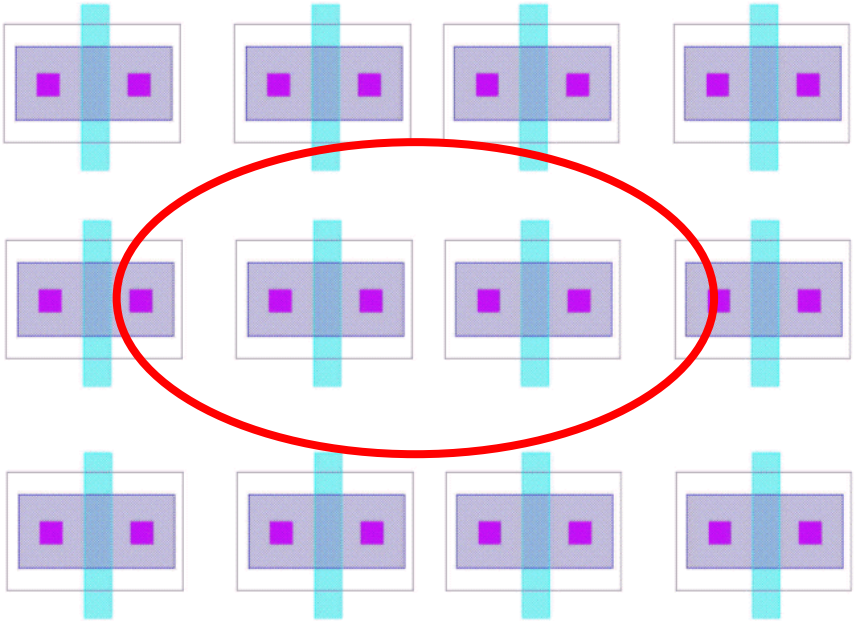
Bending gate



Matching device



Dummy cell



Layout Concept & Virtuoso

- Generic CMOS Process Flow
  - Deep sub-micron(feature size<0.25um) process
  - Process technology
- Basic Layout Concept
- Layout and Devices
- Layout Design Consideration
- Layout tool—Virtuoso
- I/O PAD

佈局規劃與步驟

- 佈局係定義各元件的位置大小及相關的連線
- 佈局的設計應考量製程的變異對電路特性的影響
- 為確保電路工作的獨立性及正確性，適當加入隔離及遮蔽功能之電路或架構

佈局設計通常包含：

1) Block partition
2) Block placement(Pin location and orientation)
3) Device placement and connection
4) Block connection
5) I/O Placement and Connection

佈局設計次序

- Device floor-planning and placement
  - Symbolic draw the transistor placement and routing channel
- Device definition and connection
  - Draw THIN + POLY for transistor definition
  - Draw Metal + Contact for device connection
  - Draw P-Implant / N-Implant for NMOS/PMOS Source/Drain
  - Draw Well for Completeness

佈局設計考量事項(1)

- 佈局設計之考量因素
  - 降低元件特性變異
    - 保持元件參數值的變化量在適當範圍
  - 保持元件間之匹配
    - 使相關元件具同樣之變化趨勢(如溫度、幾何環境相似，隔離，接觸點等)
  - 降低雜散效應值
    - 縮短信號線長度，減少耦合電容

佈局設計考量事項(2)

- 佈局設計之考量因素
  - 提供充裕之current density margin
  - 注意雜訊之隔離
    - Signal shielding, device isolation
  - 減少整體晶片之面積

About layout design

1) Package leadframe, pad location, and pad pitch
2) Floorplanning--the exercise of arranging blocks of layout within a chip to minimize area or maximize speed
3) Power distribution
4) Balance clock-tree branch
5) Latch-up
6) ESD(electrostatic discharge)
7) Antenna effect
8) Metal stress relief
9) Electromigration
10) I R drop
11) Signal coupling
12) Shield sensitive and interference-producing parts
13) Prevent coupling the clock line of digital circuit with signal lines of analog circuit
14) Metal option
15) Add probe window?

Preparing MT Form for Mask Tooling

I. Customer Information (Vendor)

1. Customer Name: _____ **2. Name of Project Leader:** _____

3. Test Chip/Product Name: U18_92E **4. Reserved Bus Code:** _____

II. Tape Out Information

5. UMC process specification check: (Please specify the spec. & version used for this tape out)

EDR spec. No.	G-02-MIXEDMODE/RFCMOS18-1.8V/3.3V-1P6M-MMC-EDR	Version No.	Ver.1.2_P2
TLR : spec. No.	G-03-MIXEDMODE/RFCMOS18-1.8V/3.3V-1P6M-MMC-TLR	Version No.	Ver.2.2_P1
INTERCAP : spec. No.	G-04-Logic18-1P6M-INTERCAP	Version No.	Ver.1.1_P1
SPICE Modeling : Spec. No.	G-05-Logic18-1.8V-GenericII-SPICE	Version No.	Ver.1.2
DRC command file:	Spec. No. 0F-MIXEMODE_RFCMOS18-1.8V-3.3V-1P6M-MMC-Calibre-drc-2.2	Version No.	Ver.2.2_P2

**UMC has the right to refuse shuttle entries if this section is not completed clearly.*

6. Database Information: (UMC FTP account name: _____)

File Name: u18_92e.db.gz File Size: 14,408,245 bytes

Grid size: 0.01 um

Name of Top Cell: u18_92e Min. Poly Gate Width: 0.18 um

Do you need UMC to shrink your database ? ☐ Yes , _____ % ☑ No

7. Data Window: Left_Bottom:(0 ; 0.015) um Right_Top:(4999.995 ; 4999.99) um

8. Are any IP/Libraries used in this test chip? ☑ NO! ☐ Ye , please fill up the questions below:

☐ **1) Standard cells used**

Vendor: _____

Library version: _____

TLR version:

9. Process : 1P6M Top metal thickness: ☐ 8K (standard) ☑ 20K (thick top metal request)

10. XX also requires Dummy / OPC patterns:

1) Please note that XX does not accept customized OPC or Dummy patterns for shuttle tape-out.
If there are any concerns, customers may add blocking layers into the GDS file before submitting.

2) XX will add dummy pattern by default. Please refer to mask tooling rule for dummy_block layers definition.
(Ref to SPEC.No.)
UMC required pattern density: Diffusion > 10%, Poly1 > 15%, Metal > 30%

3) OPC pattern will be added only for shuttles using 0.18um and beyond technologies.
Are SRAM macro used in this test chip? ☑ **No!** ☐ **Yes!**

11. Do you need XX to add the Die Seal Ring ?
☑ Yes , ☐ No, because:
☐ Seal Ring has already been added by Customer
☐ and the seal ring follows XX's standard rule. ☐ and the seal ring is customized.
☐ Not necessary.

12. Grinding Information after wafer processing:
☑ Yes , unified backlapping to final 11mil as for packaging type: BGA or QFP.
☐ No , keep original thickness as about 29mil.

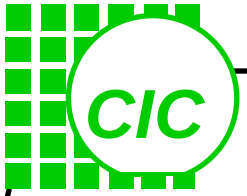
Mask Level Description		Applicant's GDS Layer No.	Mask Digitized Tone #1	Data Type #2	Notes or Instructions
Description	Mask No./Rev.				
Diffusion		1	D	0	
ASAM		*	C	0	Boolean by UMC as default.
T-Well/R-Well		n/a	C	0	Opaque layer
N-Well		3	C	0	
P-Well		n/a	D	0	
VTPL		n/a	C	0	Opaque layer
VTPHL		n/a	C	0	Opaque layer
VTNL		n/a	D	0	Opaque layer
VTNI		n/a	C	0	Opaque layer
VTNHL		n/a	C	0	Opaque layer
VTN		*	C	0	Boolean by UMC as default.
TG		37	D	0	
Poly		41	D	0	
HR		38	C	0	Opaque layer
N+		12	C	0	
P+		11	C	0	
SAB		36	D	0	
N-		*	C	0	Boolean by UMC as default.
P-		*	C	0	Boolean by UMC as default.
Contact		39	C	0	
Metal-1		46	D	0	
Mula-1		47	C	0	
Metal-2		48	D	0	
Mula-2		49	C	0	
Metal-3		50	D	0	
Mula-3		51	C	0	
Metal-4		52	D	0	
Mula-4		53	C	0	
MIM Cap		63	D	0	
Metal-5		54	D	0	
Mula-5		55	C	0	
Metal-6		56	D	0	
PAD		66	C	0	
Polyimide		n/a	D	0	Opaque layer
P-ESD*		32	C	0	Opaque layer
*P-well block	–	7	X	0	P-well block are used for MMC/RFCMOS process
N-Well Resistor	–	40	X	0	"N-Well Resistor" is to block the Diff dummy process on N-Well Resistor area

14. Special Note or Instructions from customer (vendor): Customer can add rows within item No.14 if necessary.

所有DRC Error 都是被允許的

Customer's Signature: _____ UMC Representative: _____

Date: _____ Date: _____



Layout Concept & Virtuoso

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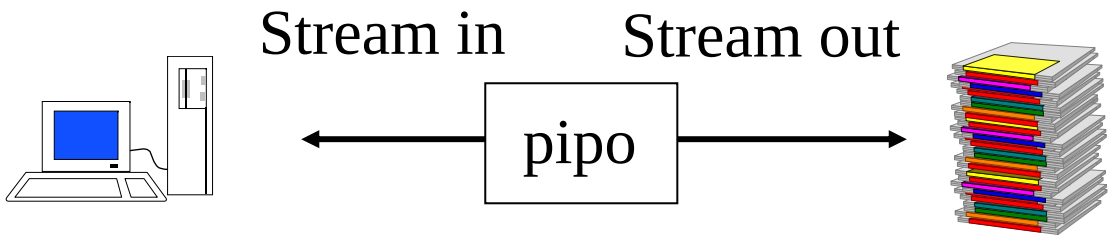
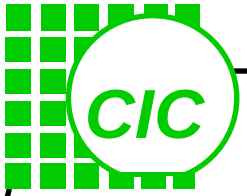
佈局檔格式與佈局輸出

- 為提供共通之佈局交換環境，因此存在幾種佈局檔格式：如GDSII, CIF,Applicon等
- 業界採用最廣之共通格式為 GDSII (Stream Format)
- 在Cadence環境中係透過 Straeam in/Stream out 來讀入/寫出 GDSII Stream data
- 而實際執行之指令為 pipo 程式

  pipo strmin *template_file_name*

  pipo strmout *template_file_name*





佈局軟體 - Virtuoso

- Shape based layout editing - Use polygon, rectangle, path, circle to define the device and connection.
- 255 definable layers for use, only part of them are meaningful to the fabrication.
- Hierarchical layout editing with edit-in-place
- Definable I/O pins for online layout verification
- Import/export layout data file to/from layout database
- Similar tools include Laker(思源) and IC Station(Mentor-Graphic)

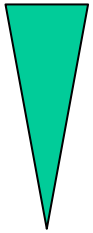
批次模式佈局驗證

- GDSII檔為設計者與晶圓廠之唯一媒介，為確保佈局檔的正確性，必須有完整的驗證步驟。
- 目前採用Dracula 或 Calibre進行佈局驗證。
- Dracula包含一系列指令群，透過前處理器的處理將命令檔內容轉換成一程序檔，佈局驗證時依程序檔之內容依序執行各項指令。
- Calibre 包含指令群與圖形使用介面(GUI)，並可透過與Virtuoso link直接呼叫
- 為求簡化複雜度，各項製程一般提供三種命令檔
  - DRC command file
  - LVS command file
  - LPE command file
- Dracula 的驗證結果可透過Dracula Interactive環境進行偵錯。
- Calibre 的驗證結果可透過Result View Environment環境進行偵錯。
- xCalibre可做LPE

Cadence Layout 設計環境

啟動layout editor 的指令有:
icfb : Full IC design environment
layoutPlus : layout editor + diva
layout : layout editor

Memory usage



開啟 layout view 時，系統需要有 display.drf 的定義，若系統找不到 display.drf 檔，或在該檔內沒有所用到的layer 定義時，則系統會提示要求merge display.drf 選擇 Tools->Conversion Tool box 項下的 Merge Display Resource Files

DFII相關檔案

Technology file : This file is a large data file that specifies all of the technology-dependent parameters associated with that particular library. Design rules, symbolic device definitions, and parasitic values are some of the technology-specific parameters common to all cells in a library

techfile.cds : The techfile.cds file contains the binary technology file

abgen.rul: A ASCII file to generate Abstract view

display.drf containing layer display information. The software reads all the display resource files, including
$ CDS_INST_DIR/share/cdssetup/dfII/default.drf
$ CDS_INST_DIR/tools/dfII/local/display.drf
$CDS_PROJECT/display.drf (if you are working in a TDM environment)
$HOME/display.drf
./display.drf

cds.lib is a file containing library definition. The software reads the first cds.lib defined in the search path file <install_dir>/share/cdssetup/set.loc.
The following is a sample listing of the search path:
./cds.lib
$CDS_WORKAREA/cds.lib
$HOME/cds.lib
$CDS_PROJECT/cds.lib & $CDS_SITE/cds.lib (if you are working in a TDM environment)
$ CDS_INST_DIR/share/cds.lib

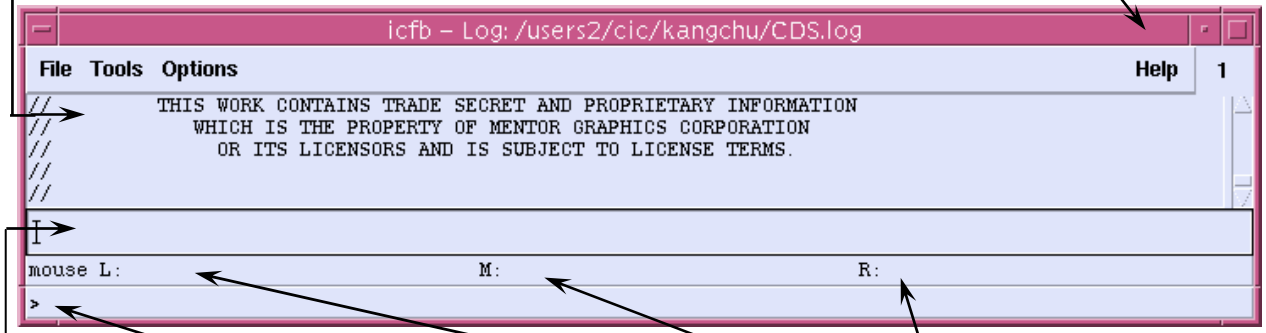
(If no cds.lib has been found, a new search path is established from the file $CDS_SITE/cdssetup/setup.loc.)

DFII中常見視窗(1)

CIW(Command Interpreter Window)

以 skill format display user 的 command 與system 的 response ,其內容亦記憶在file

on-line help

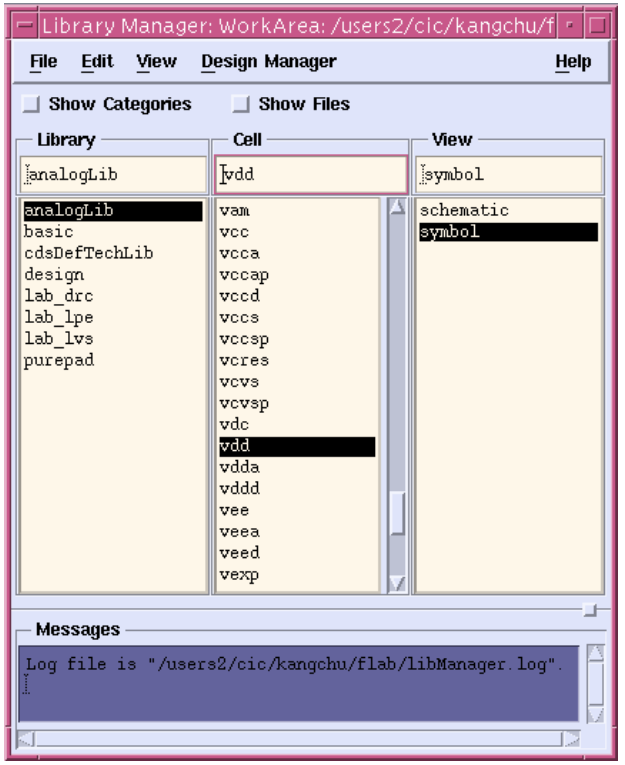


下skill command 處

提示動作

提示 mouse key 功能

Library Manager

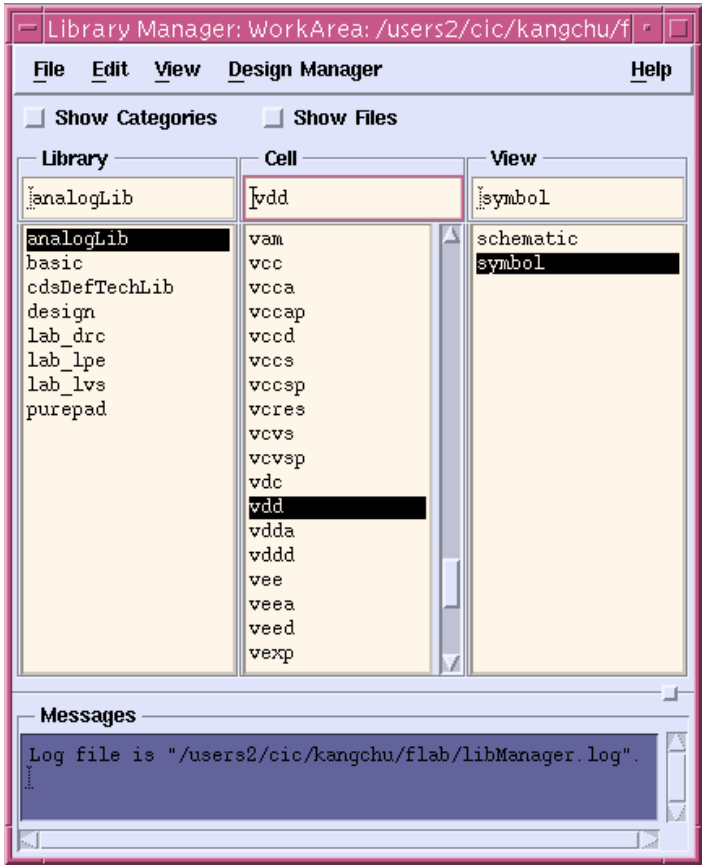


顯示的library爲cds.lib中所定義 ,這些library可被expand成cell與 cellview而 read或edit

Library Manager

cds.lib中定義了library與所在的找到的 library, 方便 user access design data, 包括create new library, cell與cell view, open或 read cellview等, 其結構 如下

Library — (Category) — cell — cellview



DFII中常見視窗(2)

不執行command並結束form

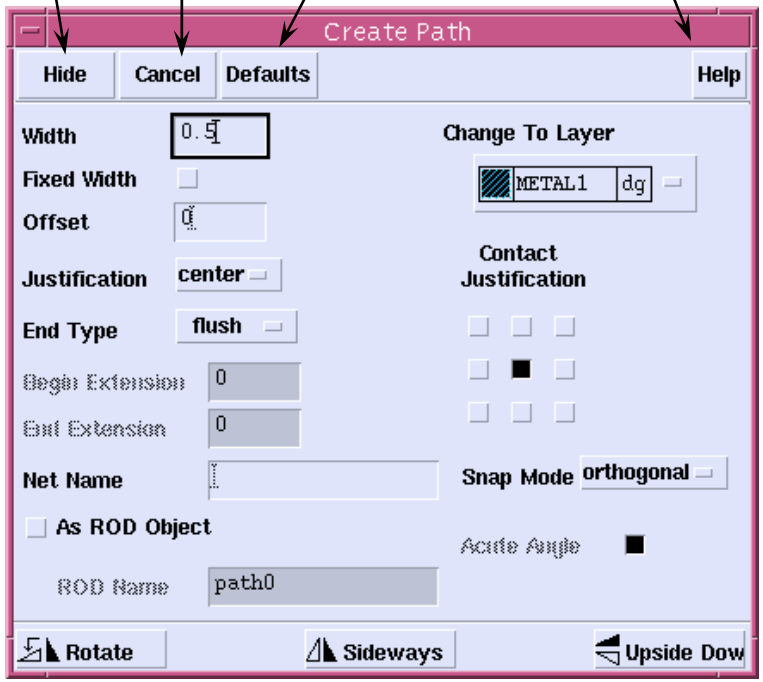
display form default值

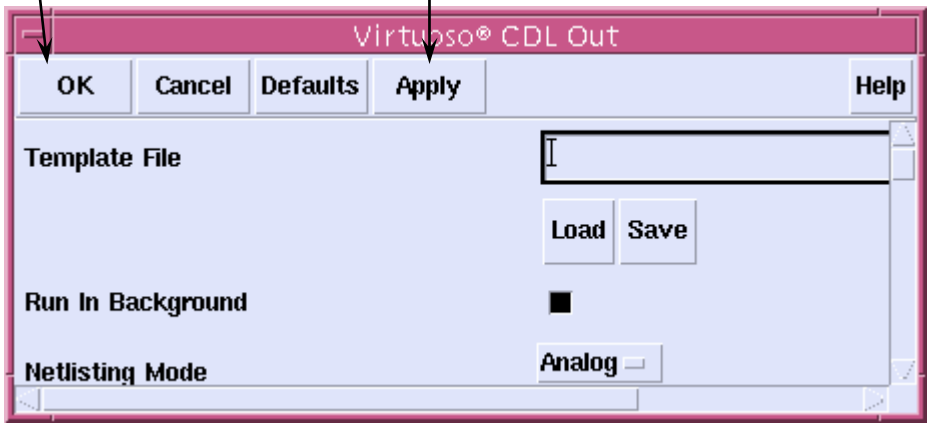
移去form

on-line help
(解釋此form用法)

執行command並結束form

執行command並保留form





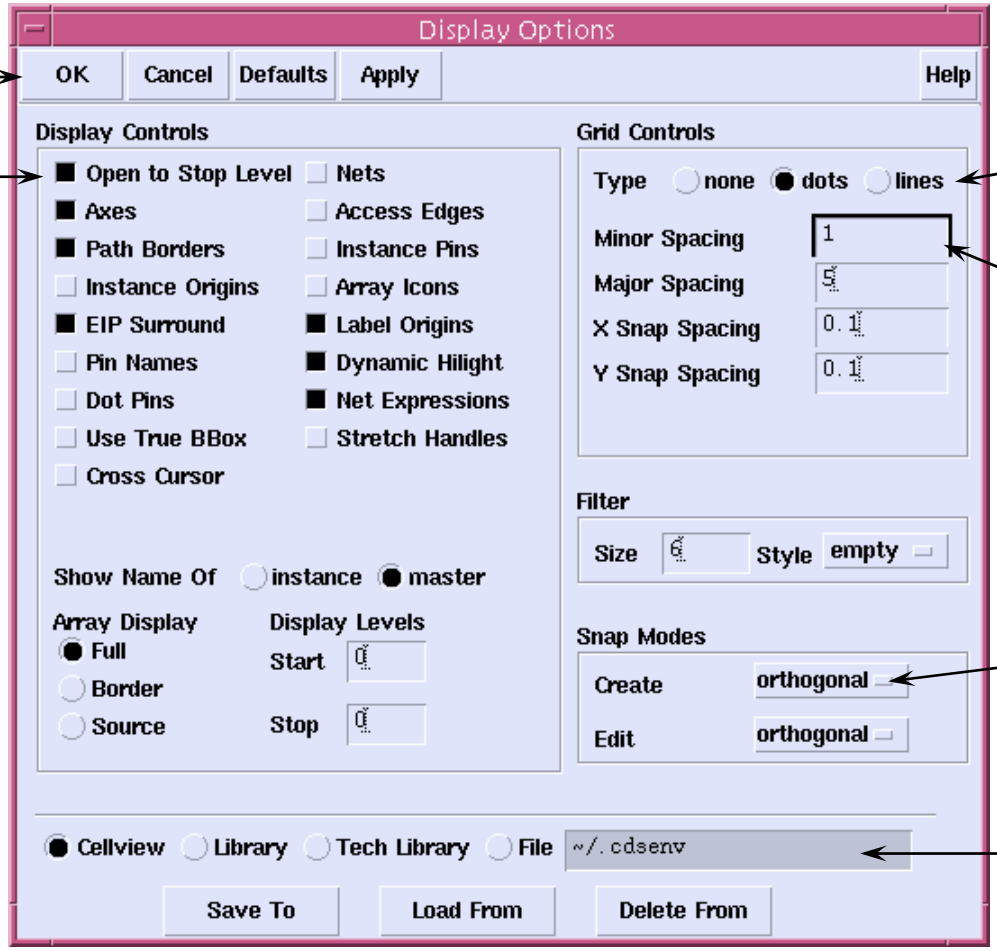
Enter key功能同OK,Escape key功能同Cancel

^a跳cursor到最前,^e跳cursor到最後

DFII中常見視窗(3)

決定form設定後
執行與否

選項



Radio Button
(只能選一項)

鍵盤 key in 處

Cyclic Field
(可下拉選項區)

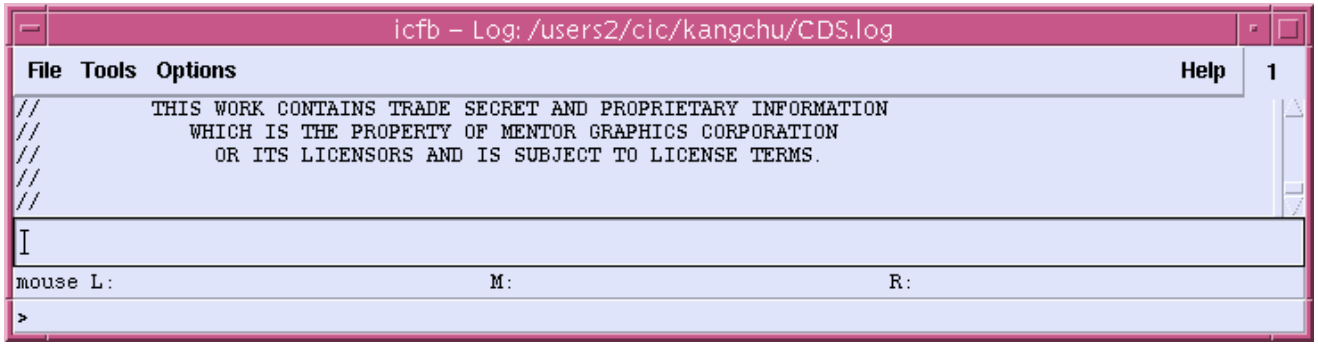
鍵盤 key in 處

Cyclic Field功能同Radio Buttons,只能選一項

開啟 CIW 視窗

在選定好製程及相關的 technology file 後, 再在 OPUS 內 create library,即可將 schematic, symbol, layout ... 等 view全建在固定 library 內

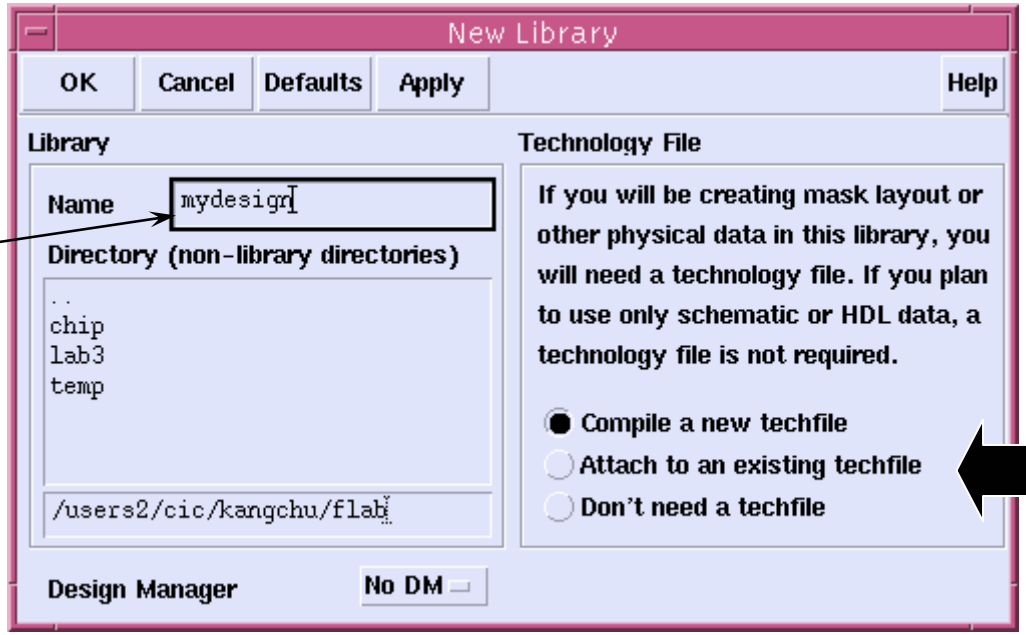
進入 OPUS
% icfb&
出現 Command Interpreter Window
(CIW)



Creating Library (1)

於CIW視窗中點選:
File -> New -> Library...

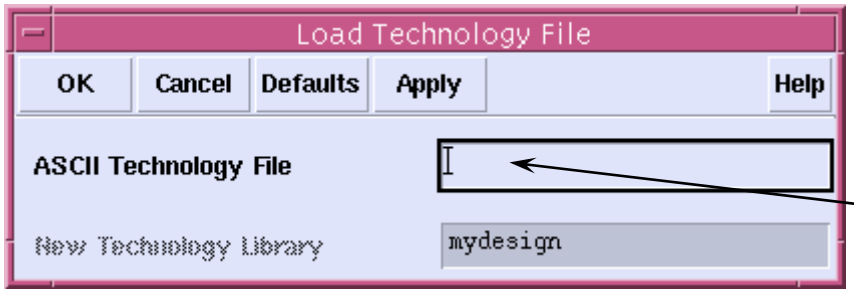
填入要新增Library的名稱



三選一

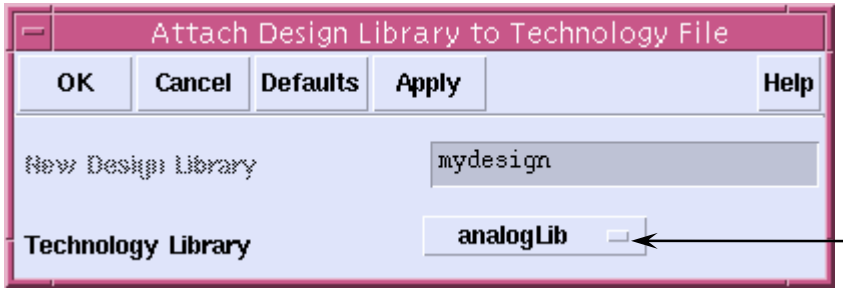
Creating Library (2)

若選取Compile a new techfile



填入technology file

若選取Attach to an existing techfile



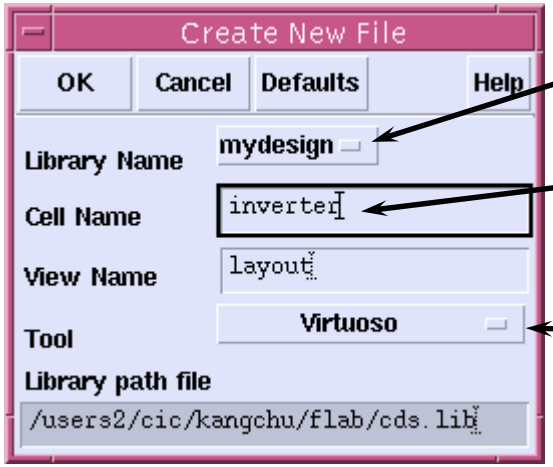
選取已存在的Library

Creating Layout Cellview

Layout Editor

在這裏將介紹 Virtuoso Layout Editor 的使用

File -> New -> Cellview



選擇 Library

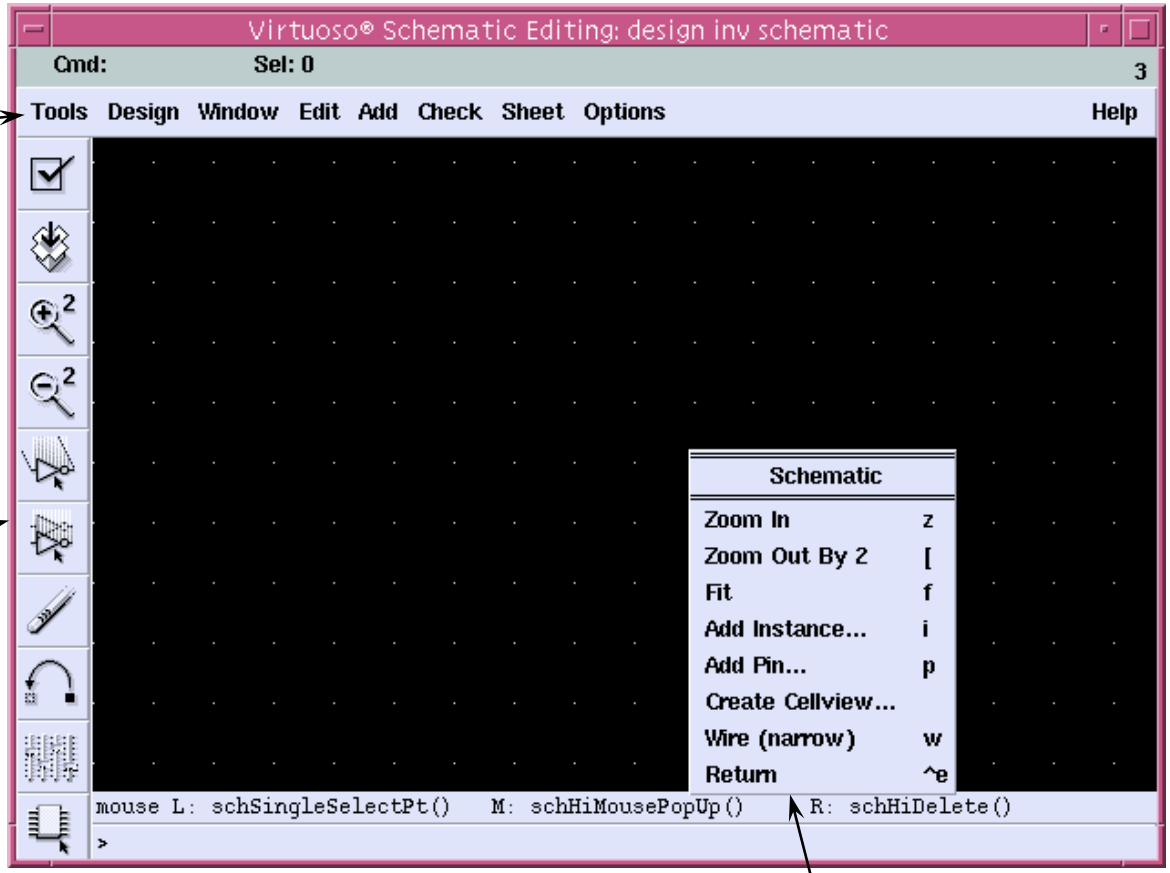
輸入Cell Name

選取 cellview 的編輯程式
在此選取 Virtuoso
此時 View Name 會自動出現 “layout”

Layout Editor Window

編輯視窗上方
爲工具列

編輯視窗左方爲
各功能的快速鍵
當滑鼠移至各功
能的快速鍵上時,
會出現各快速鍵
的說明.



加選或少選 (Shift or Ctrl)

在編輯視窗內按滑鼠中鍵
切換此 window 以方便選用

Layer Selection Window (LSW)

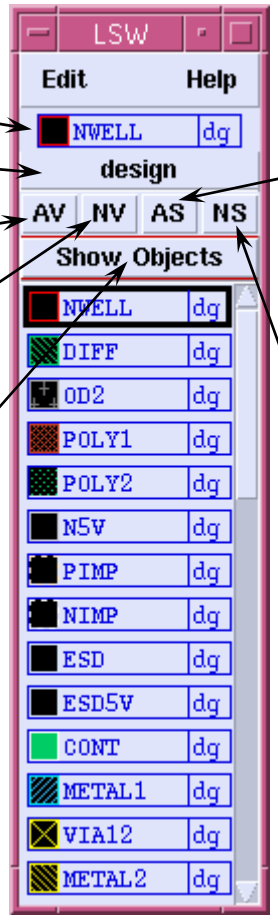
目前所選之層

library name

所有層均 show 於 layout cellview 中

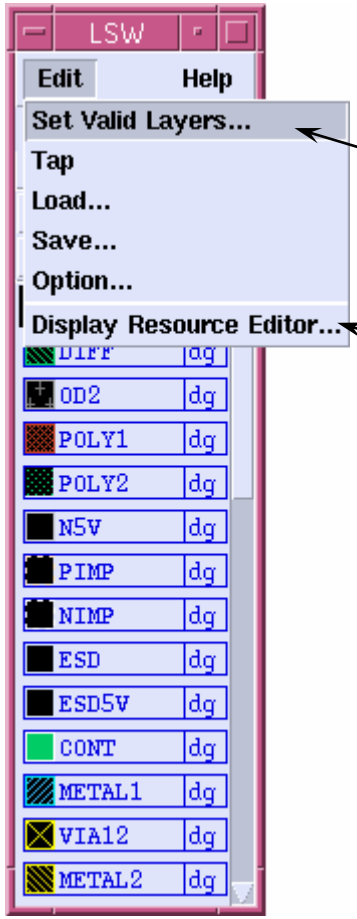
除目前所選之層外在 layout cellview 中均不顯示

按下後可以設定 Instance, pin等相關物件是否可以被選取



LSW上所有圖層在layout 編輯畫面中均可被選取

所有的圖層在 layout 編輯畫面中均不可被選取

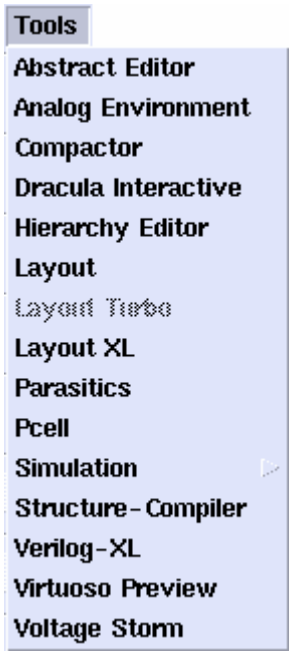


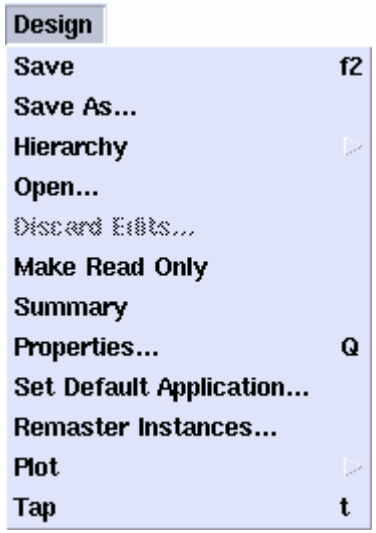
設 show於CIW上之層

設LSW上所選層顏色等

Layout Editor Menus (1)

key-in **f** 功能同 Windows > Fit All (f爲其bindkey)





layout editor 的主要選項與其相對 bindkey

Layout Editor Menus (2)

畫矩形

畫多邊形(最後一點 double click)

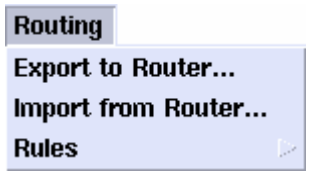
畫長條接線

畫文字 標示

將已畫好之 cell引用到此layout view

畫 pin(用以給定node name)

畫 tech. file 中已定義好之contact



Calibre 爲Mentor公司所推出之Verification Tool，可與Cadence Virtuoso做link

Edit Menu

邊緣或角落擴展

調整 object 邊緣處

砍去 object 部份圖形以調整形狀

corner 調變

擴大或縮小某 object

定分割線使object partial stretch

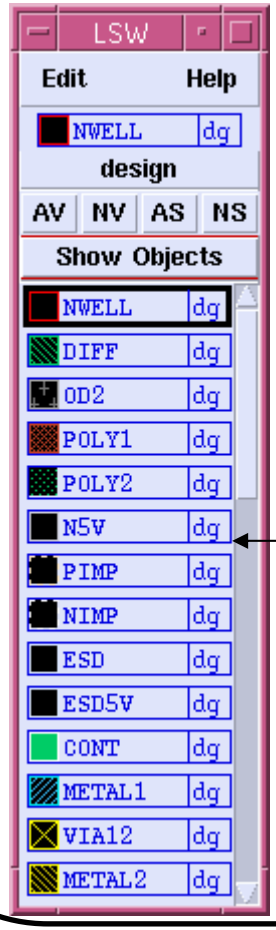
使一object 附屬到另一object,當一object move, copy, delete 時,其附屬 object 同時動作

將path, circle, ellipse,donut 等圖形轉成多邊形

Usage of Create and Edit

◆Create an object

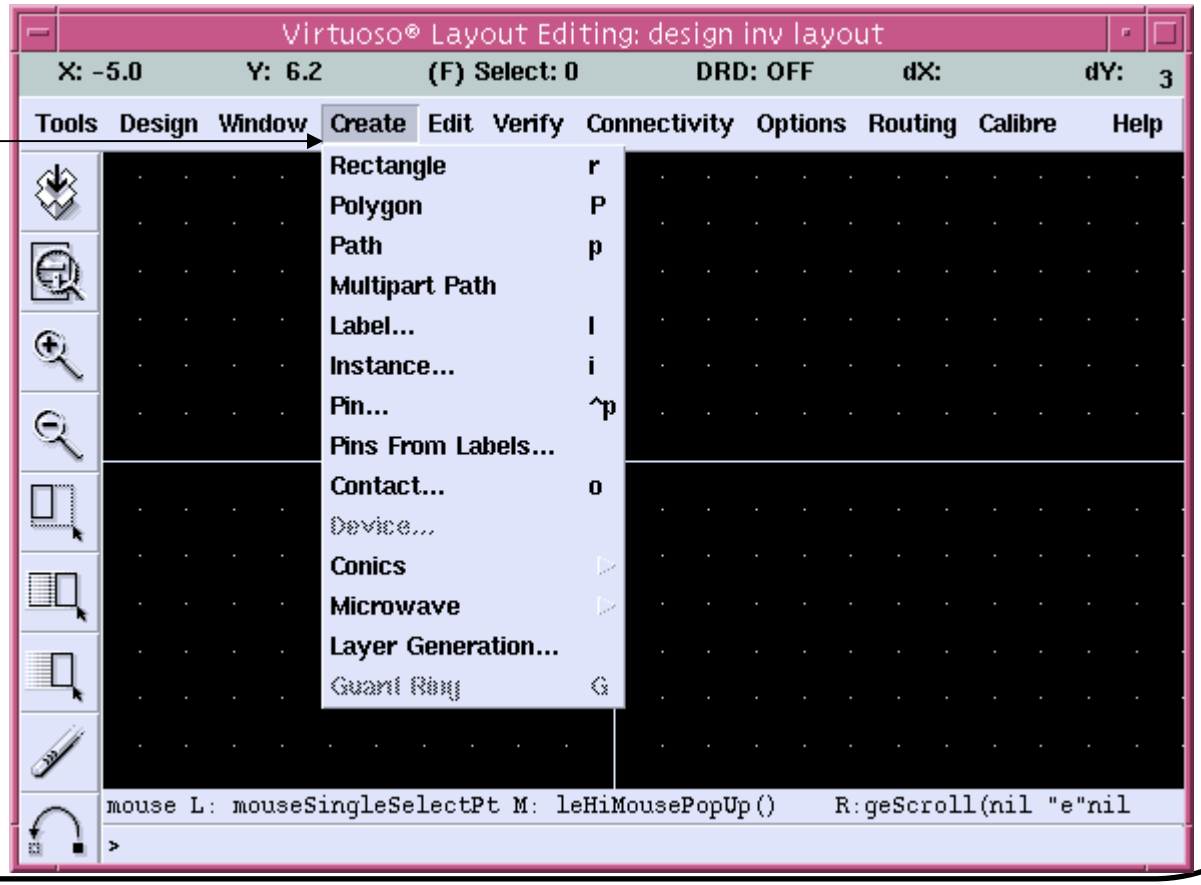
➢ Select a layer in LSW => Select what type object to create in "create" menu => Draw an object in layout editor

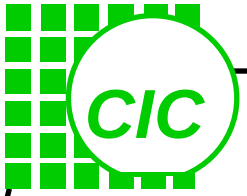


2)Select a type in create menu

1) Select a layer in LSW

3) Drawing in layout editor





Usage of Create and Edit

- Edit an object
  - i) Select an object to edit => Select what action to edit in “edit” menu => Edit object in layout editor (Action one time only!)
  - ii) Select what action to edit in “edit” menu => Select an object to edit => Edit object in layout editor (Action before press “Esc” button)

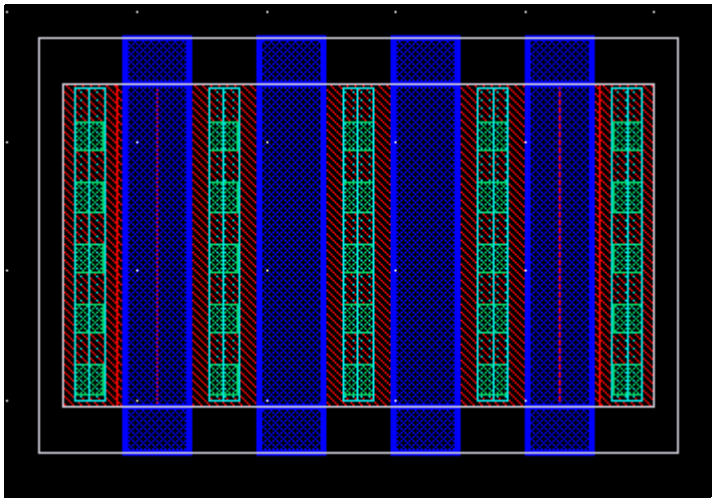
Press “F3” to set action after choose an action in edit menu

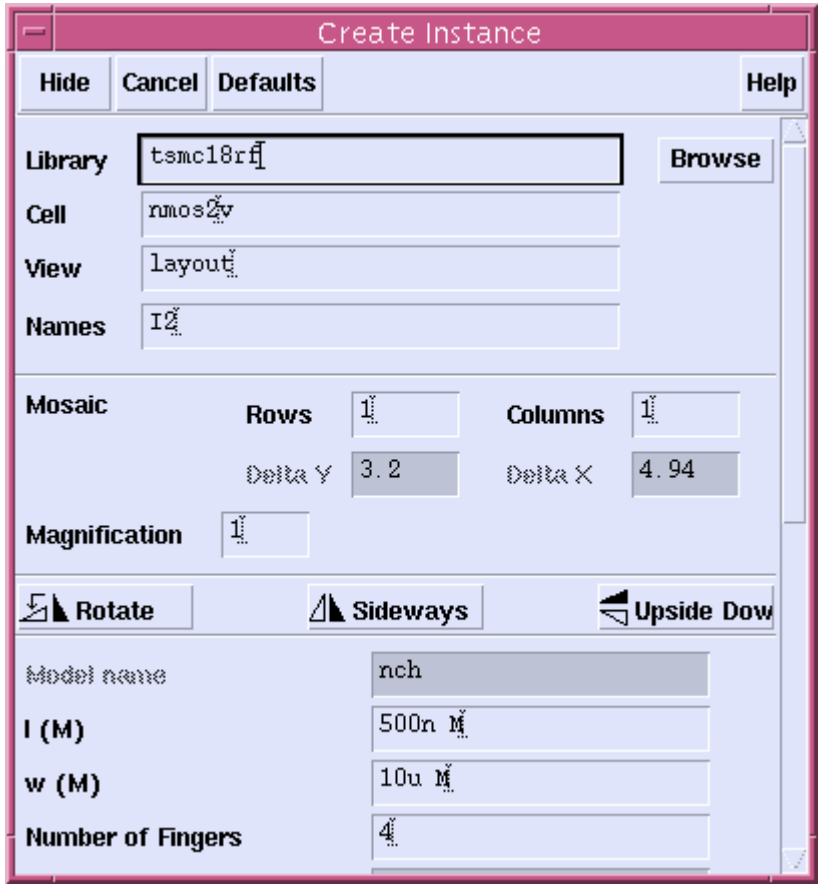
Using Pcell in Layout Editor

Pcell - parameterized layout cell

Use **create instance** menu
Specify length/width/number of Finger

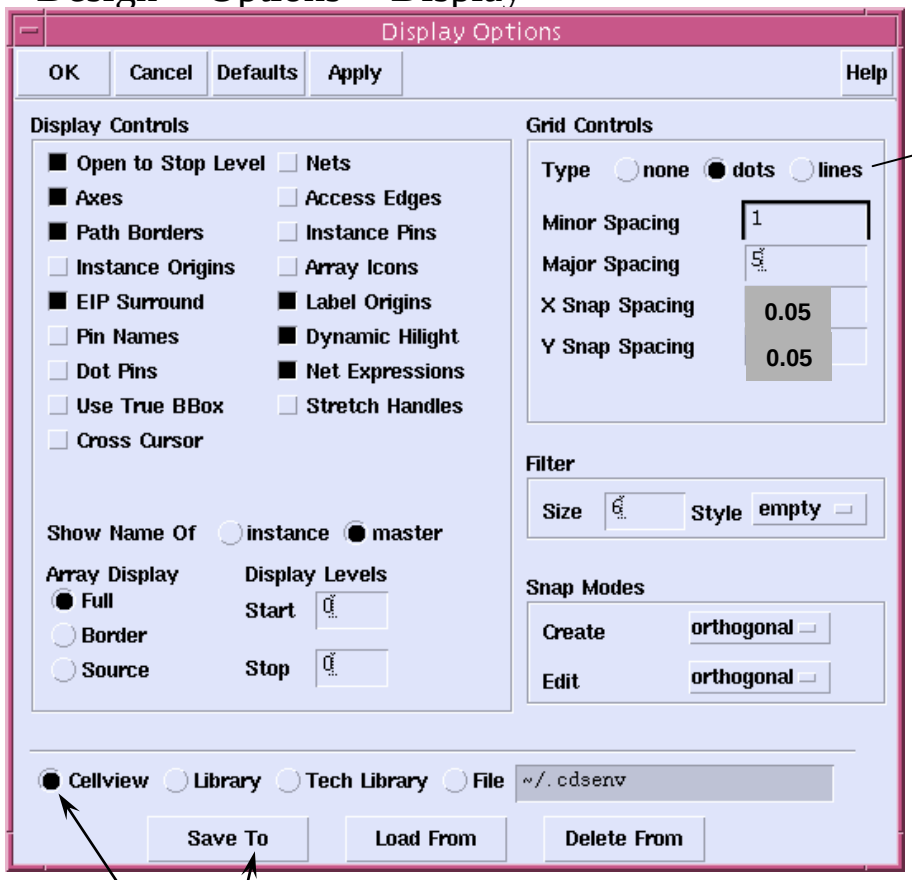
Available pcells in 0.18um process





Display Control Wndow

Design-> Options-> Display



set grid 顯示方式

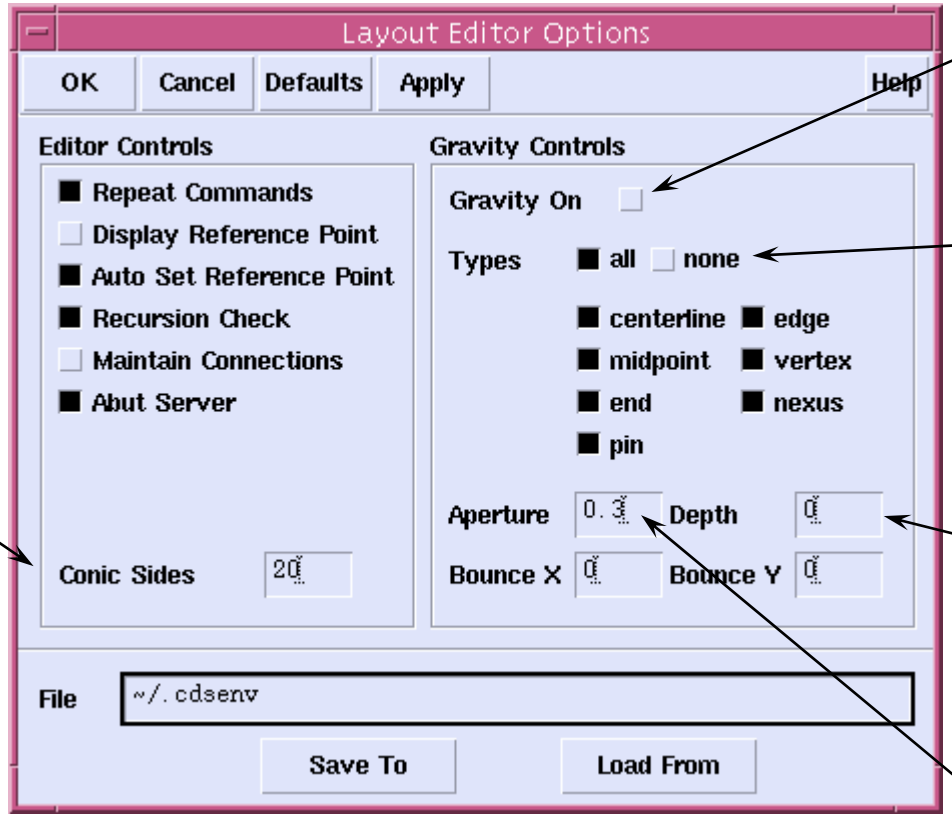
set minor grid 間距多少 user unit
set major grid 間距幾倍於 minor grid
set X 軸移動之 min. 間距
set Y 軸移動之 min. 間距
(以上二值之設定須爲design rule 之公因數)

set 畫線時 cursor 之 跳動方式(snap)
set 畫線時之限制方式

對cellView存目前設定情況

Editor Option Control Window

Design-> Options-> Editor



set cursor 靠近 object 時即被吸到 object 邊緣 (快速鍵 g 切換)

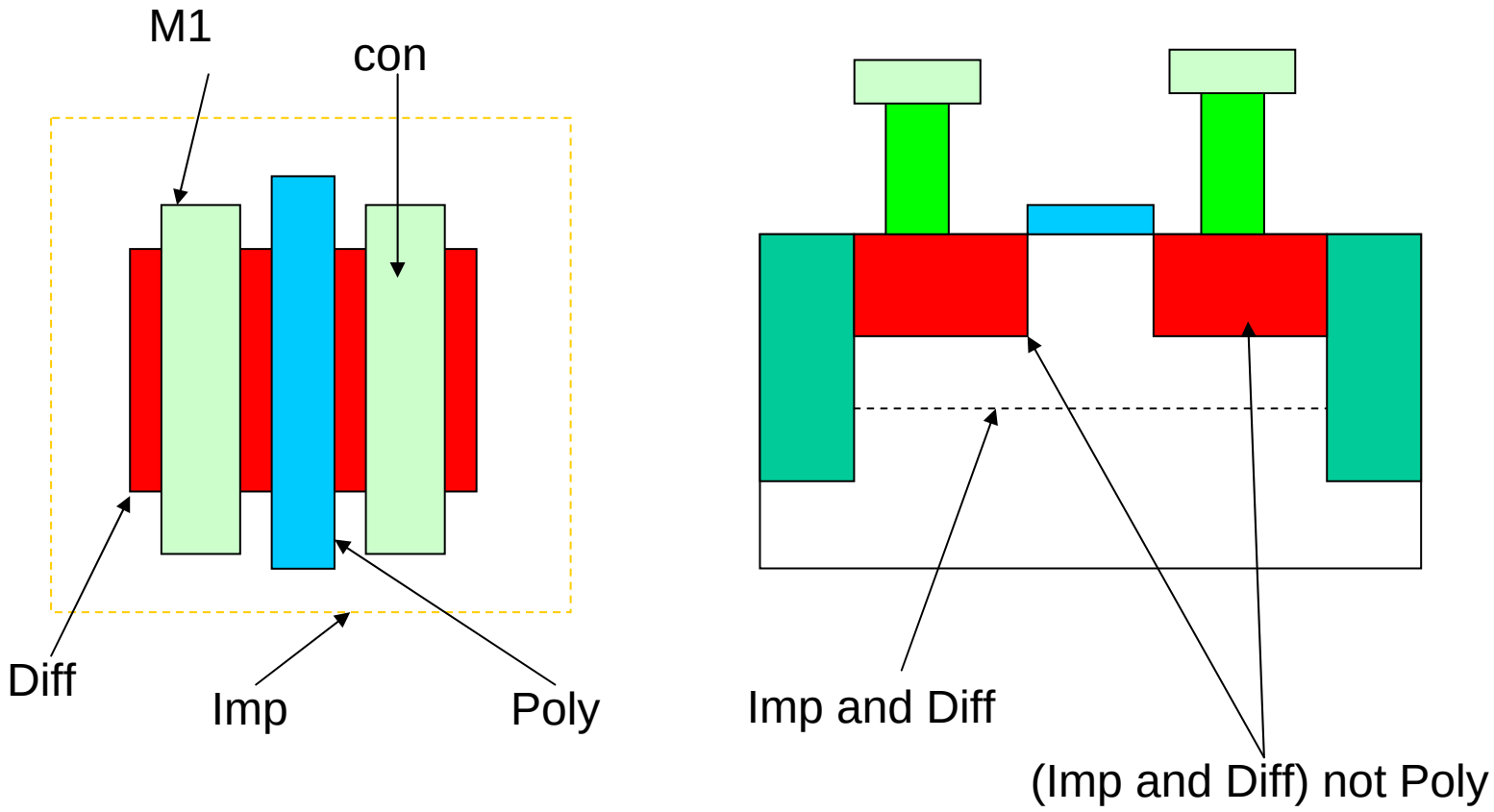
set gravity on 時所作用之 object

set conic 經過 Convert To Polygon 或 Merge 後變成幾邊形

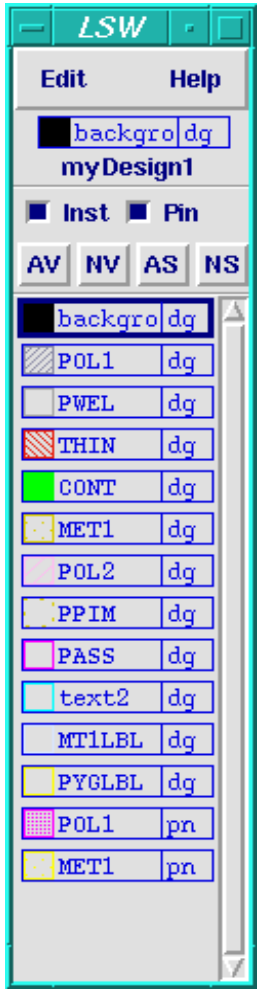
gravity作用深度

set gravity on 時能影響之範圍爲幾 user unit 以內

平面佈局與切面示意圖



Adding Label and Pin



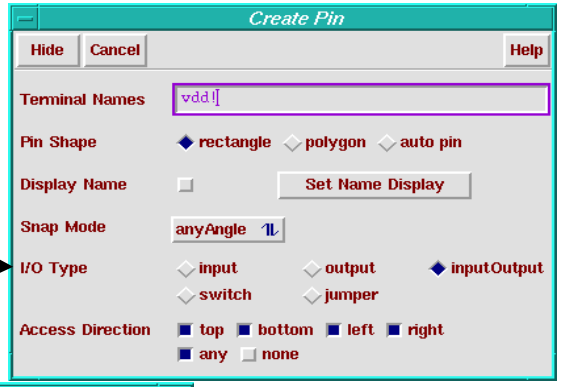
爲使 Calibre LVS check 時認 得 layout 之 port name, 在用 MET1 dg layout 之 terminal 上,選用 MET1 dg ,

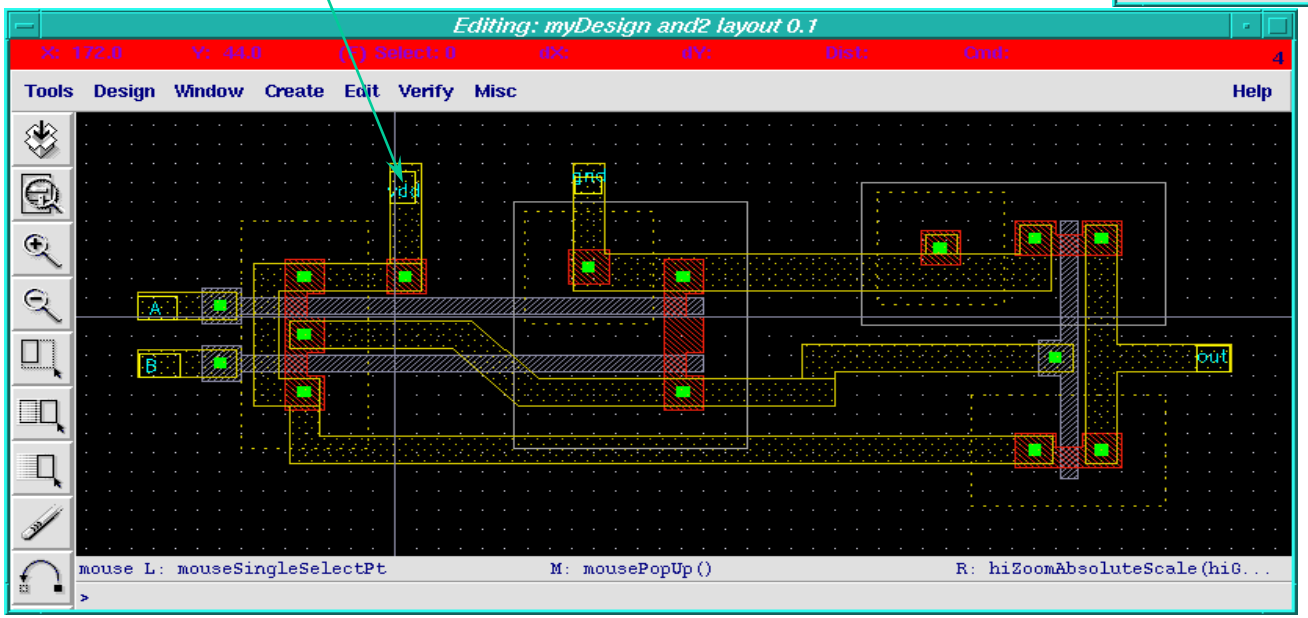
Create-> Pin...

layout一層

(note:此層將視同layout製作)

(選 適當的 I/O type)



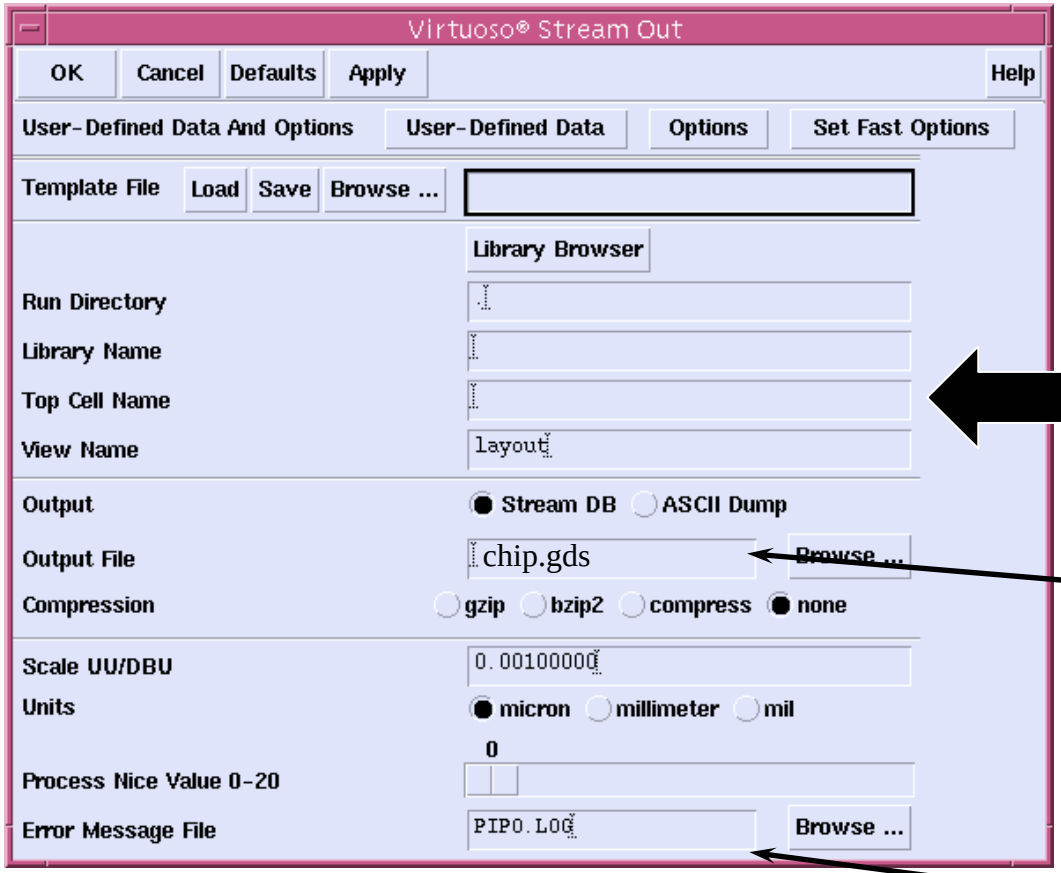


A, B, out, vdd, gnd 爲選用相對應的text

Create-> Label...標示於 terminal 上, 除爲 user 本身認知用外, 亦作爲LVS check 時的Pin (port)

Preparing Layout (GDSII)

In CIW, select File -> Export -> Stream ...



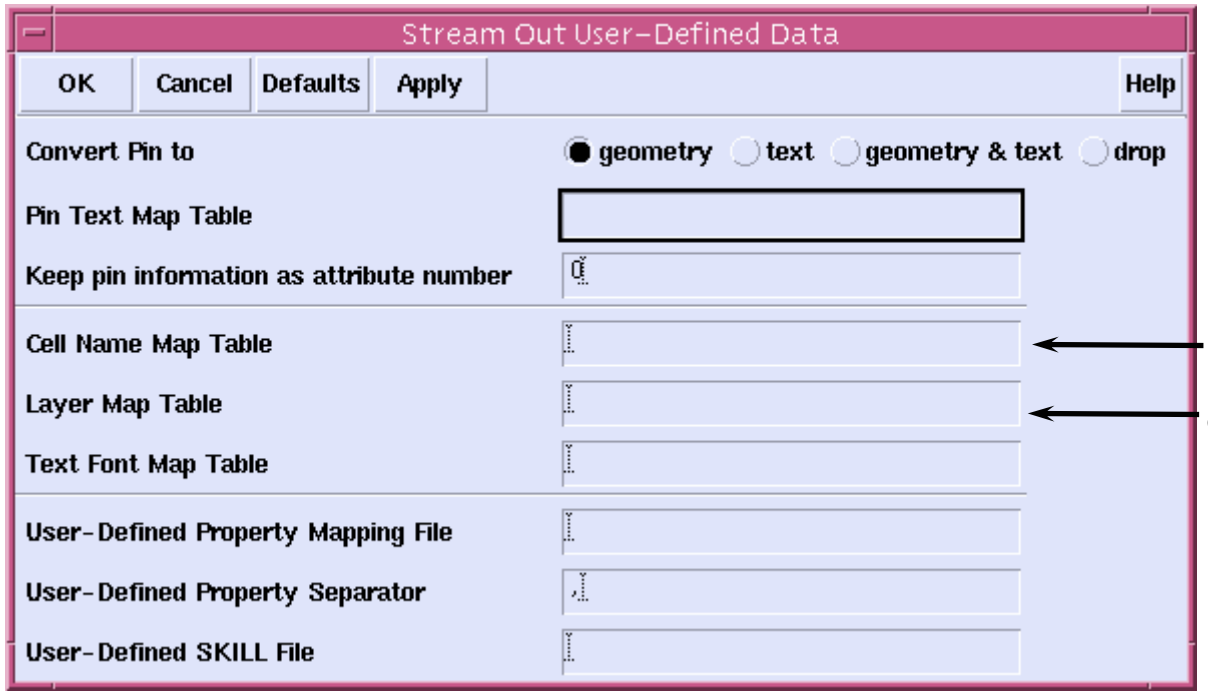
assign which layout to stream out

assign the stream-out layout file name

translation information file

Setting Specified Layer Mapping

In Stream Out form, select “User-Defined Data” button



assign the file of cell name mapping

assign the file of mapping number

Stream Layer Mapping Table

GDSII file 也稱作Stream-format, 當你在CIW選擇Translators ->Physical ->Stream Out 時, 則出現如同上圖的表格, 其中經常使用的選項是:

(1).Library Name = (myDesign)是你在Opus系統中的Library名稱

(2).Top Cell Name = (top)是你在Library中最上層cell,top cell 在Dracula 亦稱primary cell

(3).Output File = (top.db) 是寫到disk中GDSII file名稱

.Layer Map Table = (layer.map)通常是空白不使用, 若須轉出非本 technology file 定義的 layerNubmer時,則編輯layer.map檔案格式如下:

```
;
;Opus_layer_name  layer_purpose  Stream_layer_no  Stream_data_type
;
  POLY              drawing          6                0
  MET1              drawing          12               0
;
```

以上二列的作用, 對Stream Out而言,是告知OPUS將POLY層轉出為layer 6, 將MET1層轉出為layer 12.(在Stream In時也可用此mapping file,以告知OPUS POLY 取layer 6, MET1取 layer 12).

Stream Out實際上是呼叫PIPO(Physical In,Physical Out)執行,所以當你執行完 Stream Out, 程式後會自動產生PIPO.LOG檔案,PIPO.LOG是執行過程的摘要,統計資料包括(1)Top Cells ,(2)List Hierarchy,(3) Individual Cell 內容(4) 各Layer統計.

在Opus technology file中有定義layerName及layerNumber,layerColor,layerPattern,但是GDSII(top.db)中只有layerNumer(0-63),確定Opus technology file中的 layerName與GDSII layerNumer的對照, 以便在用Dracula讀layerNumber及送交光罩公司 MT-form時不致發生layer不相吻合的錯誤.

Layout Concept & Virtuoso

- Generic CMOS Process Flow
  - Deep sub-micron(feature size<0.25um) process
  - Process technology
- Basic Layout Concept
- Layout and Devices
- Layout Design Consideration
- Layout tool—Virtuoso
- I/O PAD

I/O Placement

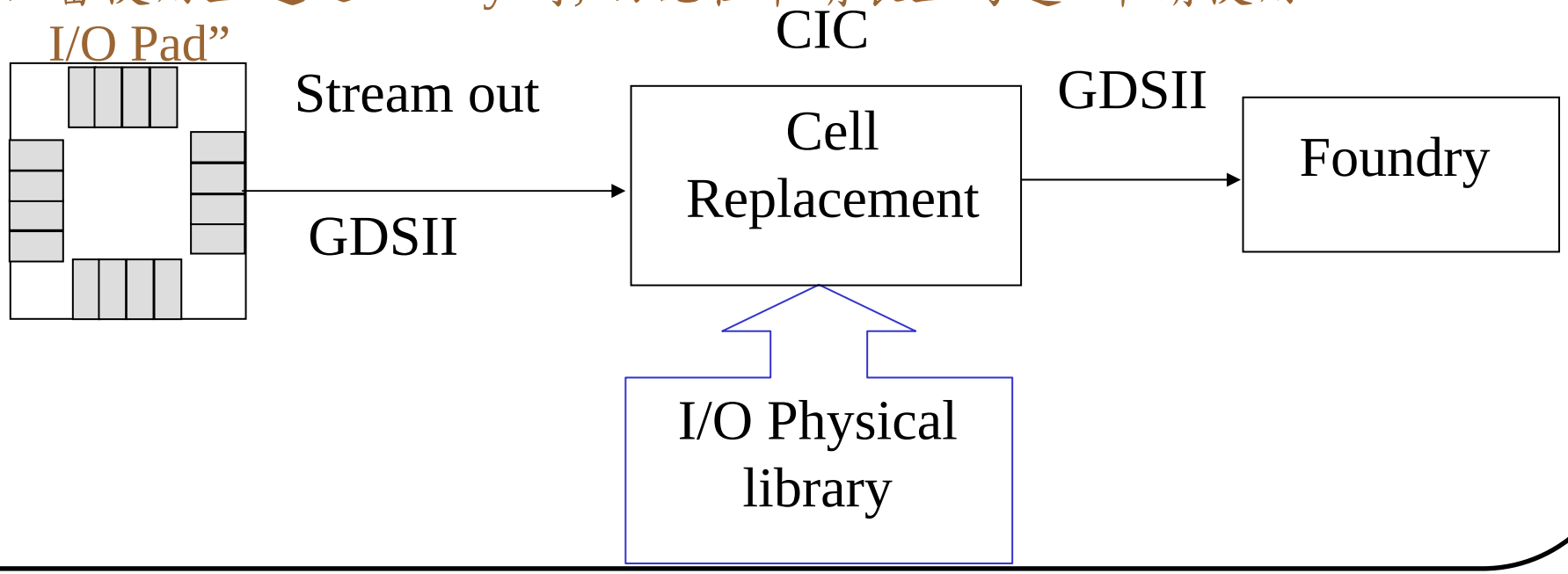
- 為提供封裝接腳到晶片內部的連線，需加上PAD
- 為提供足夠的驅動能力在output pad前通常加上驅動電路
- 為提供內部電路的保護，在input pad後加上保護電路。
- 為提供晶片外部及晶片本身訊號位準的相容性，input pad 後可加上level shifting 的電路。
- 為提供驅動電路及保護電路的電源，I/O pad處需有電源，為避免內部電路受I/O 訊號的干擾，I/O 電源及 CORE 電源最好分開。
- Output pad 因需提供較大的驅動能力，因此一組power最好只供應不超過 8 個會同時動作的輸出。
- 為求偵錯的便利性，可在需要觀察的訊號上加上 probing window(即加上 PASS 層)。
- Isolation and protection
  - –Add enough Well contact/ Substrate contact
  - –Add guard ring

The I/O Supported by CIC

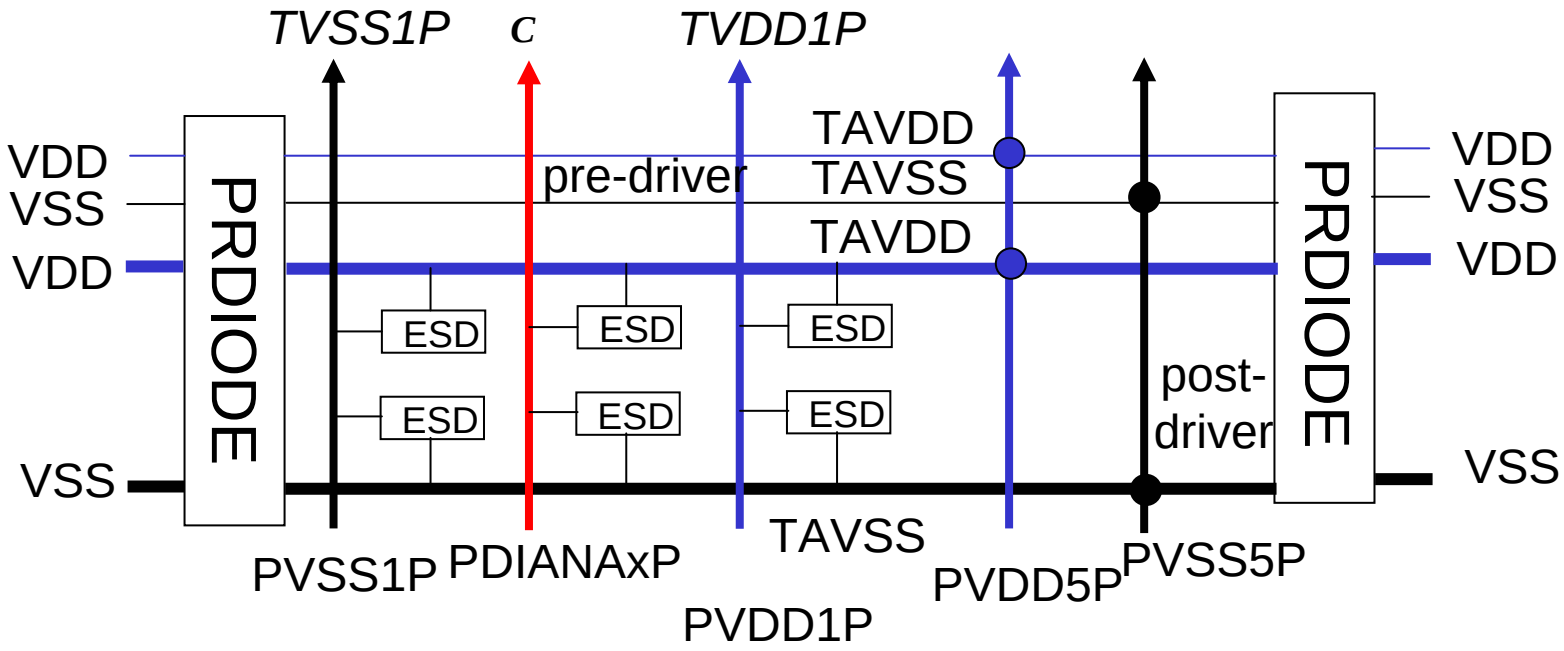
一般我們將chip的internal circuit部份稱為core, 而pad部份(包括power, ground, input, output)稱為 I/O, 無論是core或 I/O部份的電路, 都得注意 latch-up問題, I/O部份的電路須作ESD protection. 在process data中一般還包括這些避免latch-up與ESD的design rule,若有已驗證過且合本身design需求的I/O pad, 最好直接引用.

PAD Usage

- User 必需依Pad的使用手冊中,從pad library自行選擇所需的pad cell, 並完成 PAD 的wire routing
- User 的cell name 不能和 I/O cell 的cell name相同(TSMC 0.35um 2P4M CMOS製程)
- 當使用上述之 library 時, 切記在申請表上勾選“申請使用TSMC I/O Pad”



Analog I/O Pad Structure



PRDIODE : provide isolation of digital/analog I/O power rings
PVDD3P : VDD for core/ pre-driver/ post-driver
PVDD1P : VDD for core ; PVDD1P1 : VDD for core using with PVDD2P
PVDD5P : VDD for pre-driver/post-driver
PVDD4P: VDD for pre-driver
PVDD2P: VDD for post-driver

PAD Construction

- 在沒有提供PAD的情況下，則需要自行畫PAD