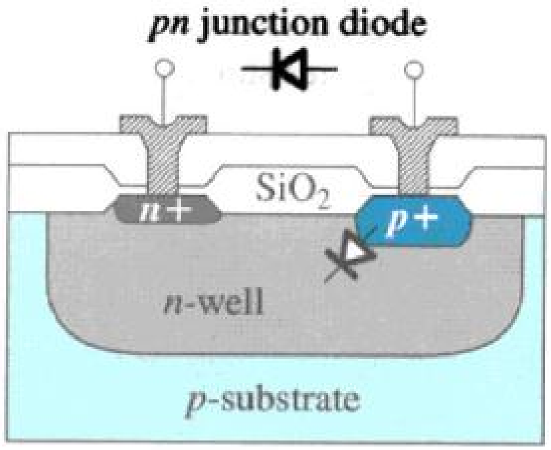
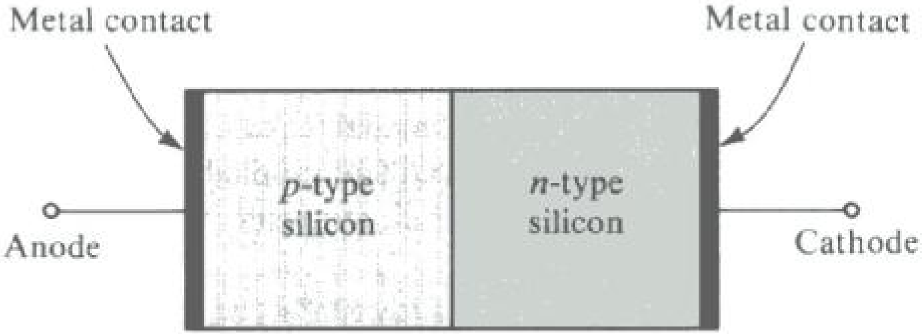
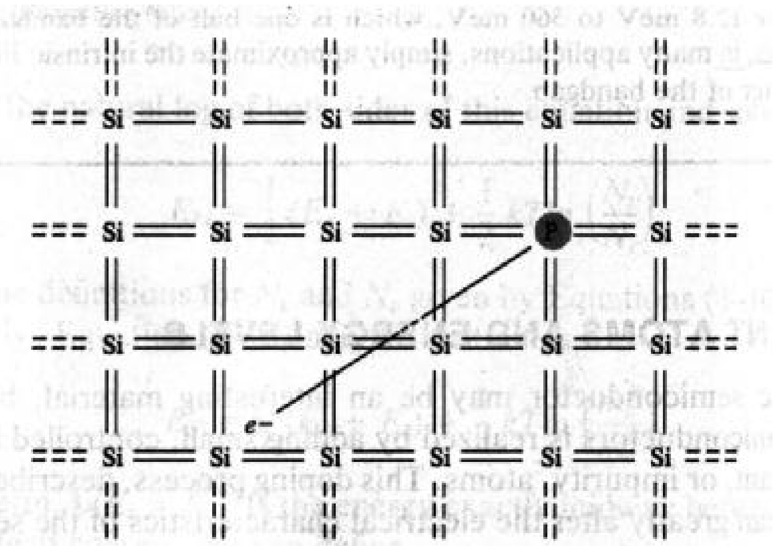
Chap 3. P-N junction

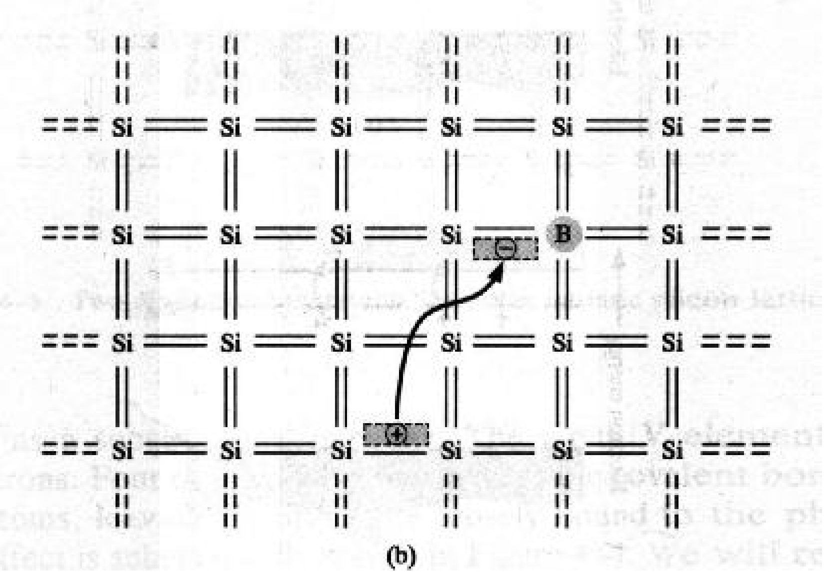
- P-N junction Formation
- Step PN Junction
- Fermi Level Alignment
- Built-in E-field (cut-in voltage)
- Linearly Graded PN Junction
- I-V Characteristics
- Breakdown

Basic Symbol and Structure of the pn Junction Diode

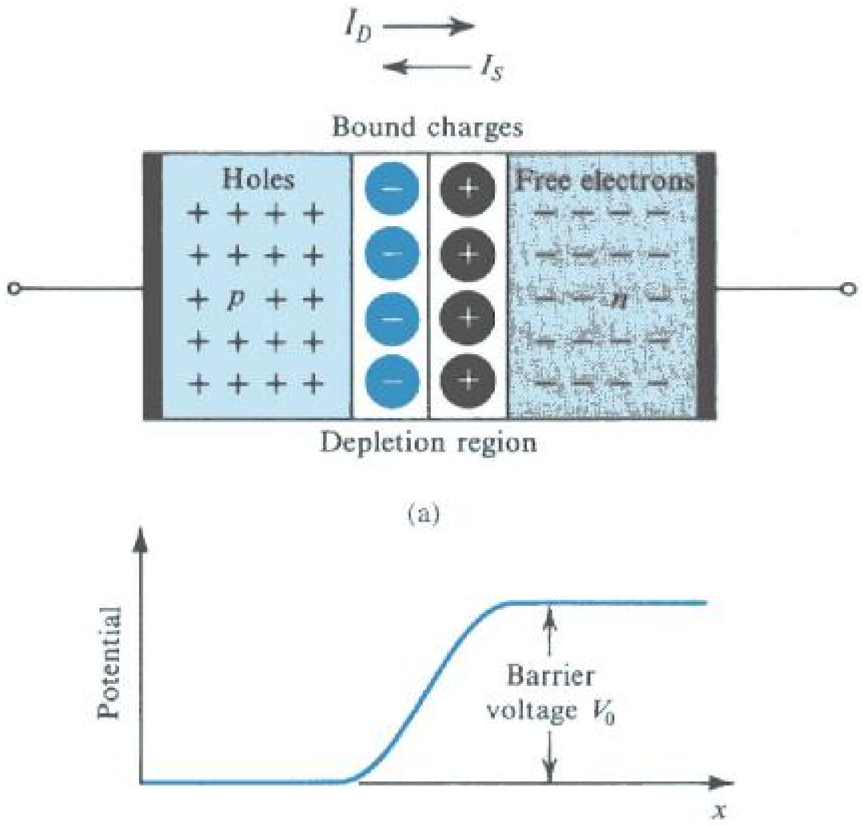


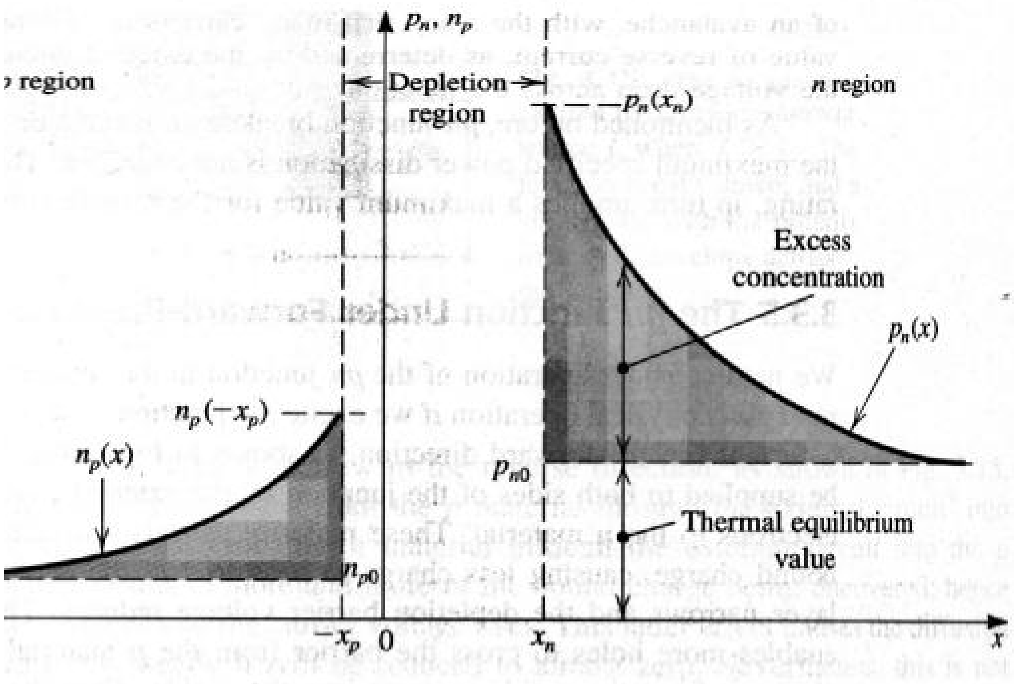






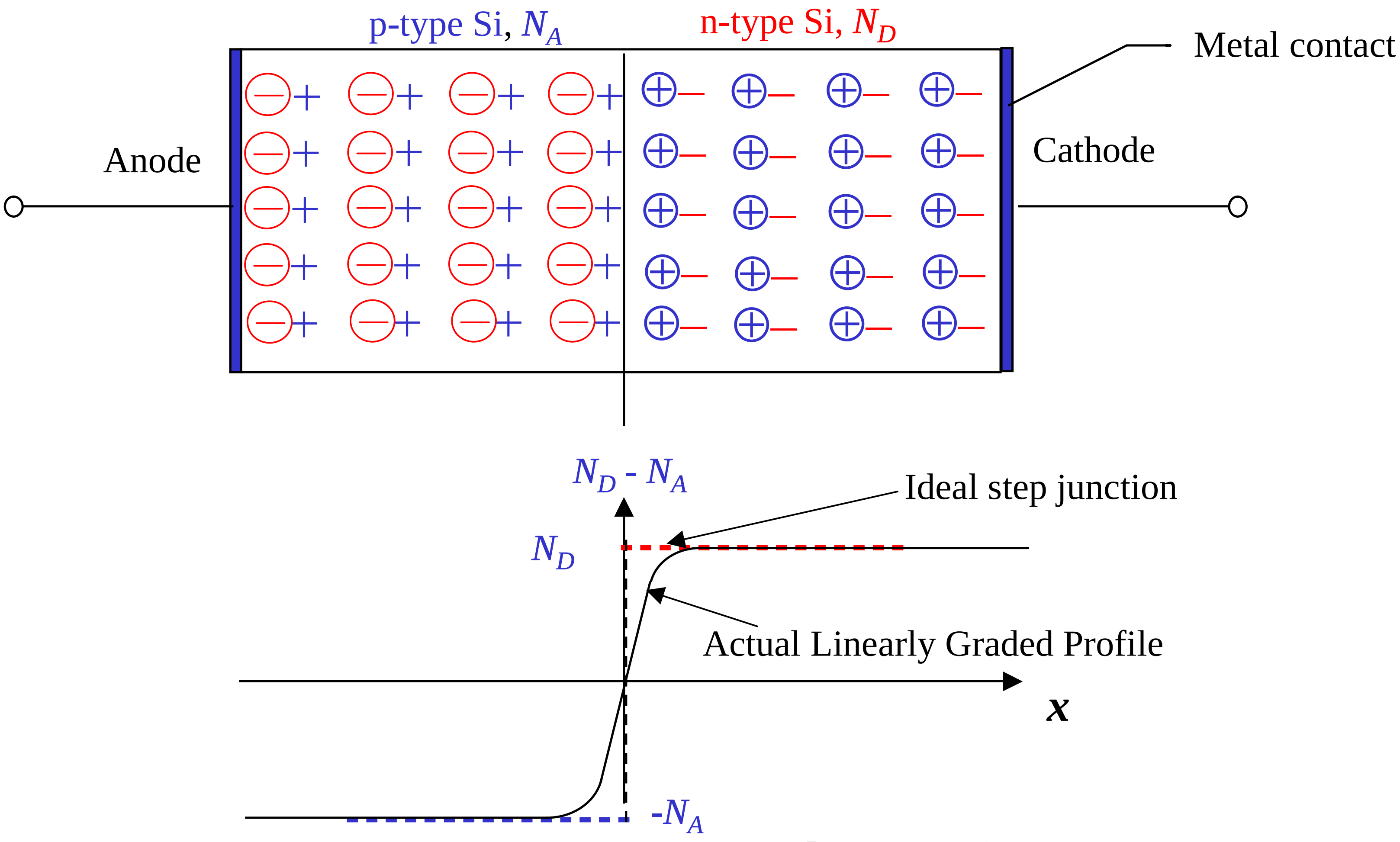
Charge Distribution across PN junction



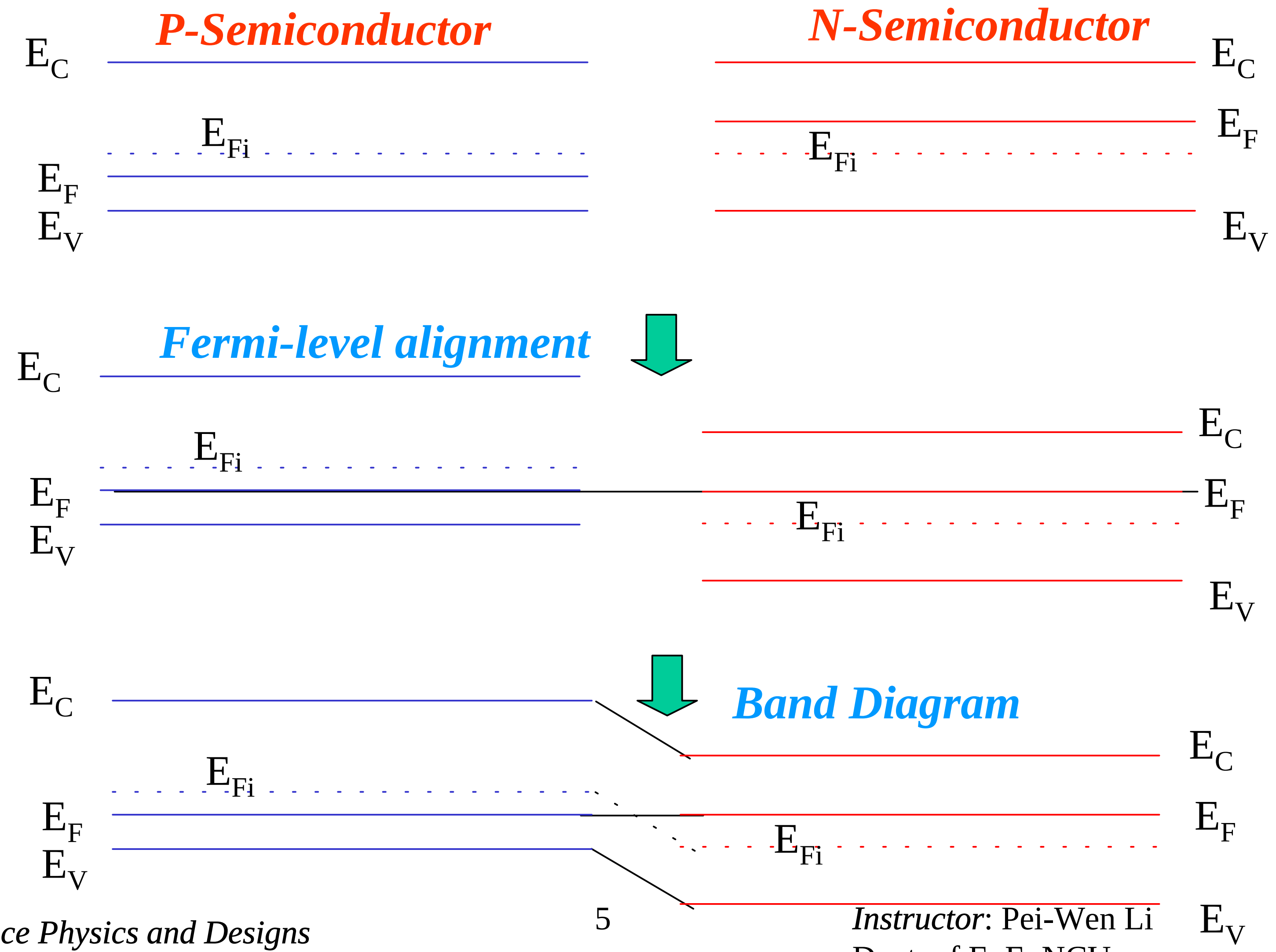


ority-carrier distribution in a forward-biased *pn* junction. It is assumed that the *p* eavily doped than the *n* region; $N_A \gg N_D$.

Step Junction



Step P-N junction—Band Diagram


P-Semiconductor

N-Semiconductor

Fermi-level alignment

Band Diagram

Step Junction

- Recall Poisson's Equation:

$$\nabla \bullet E = \frac{r}{k_s e_o}$$

r : charge density

k_S : dielectric constant

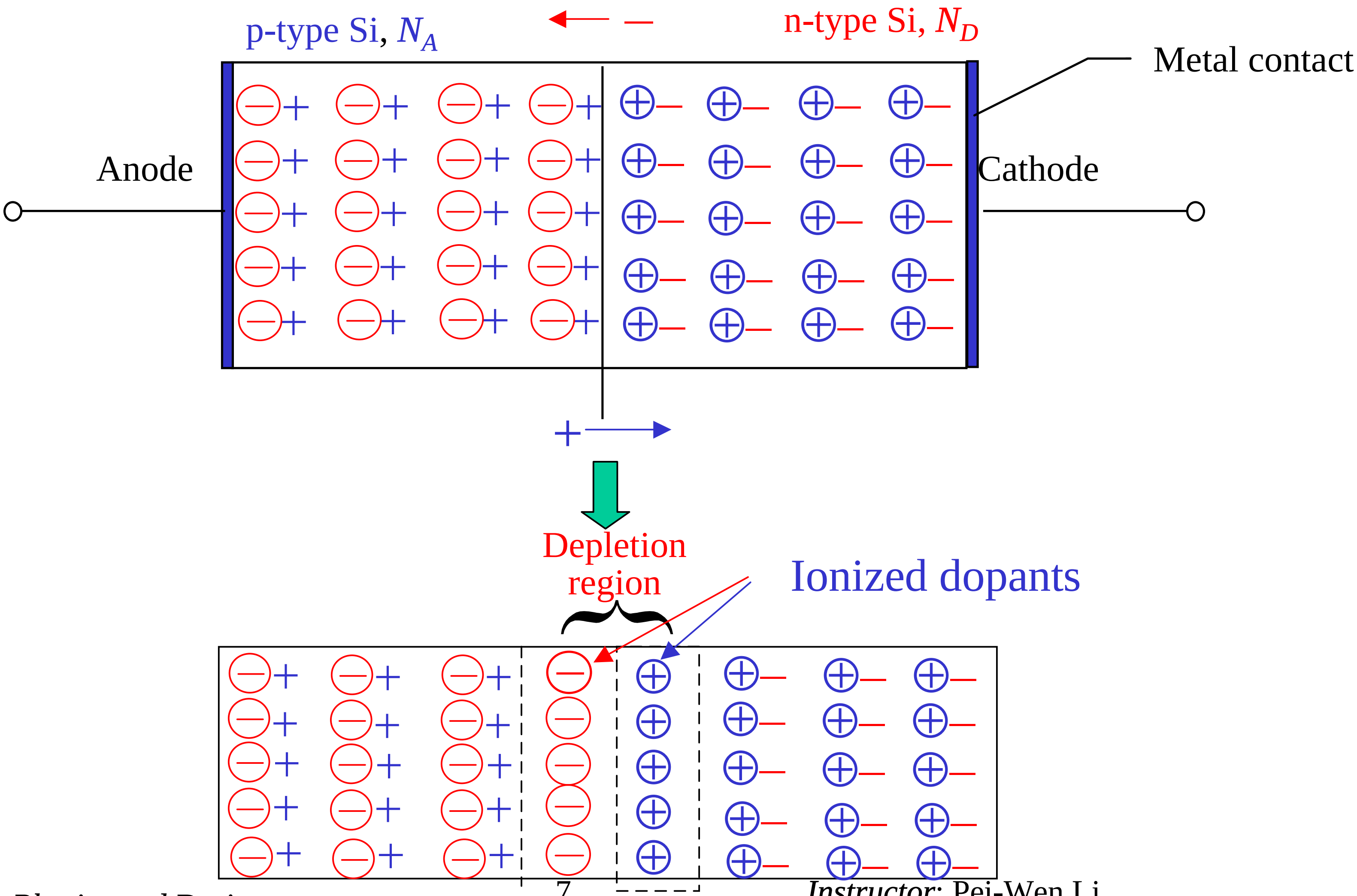
- For 1-D, $E = E_x$

$$dE/dx = r/k_s e_o$$

where $r = q\,(p - n + N_D - N_A)$

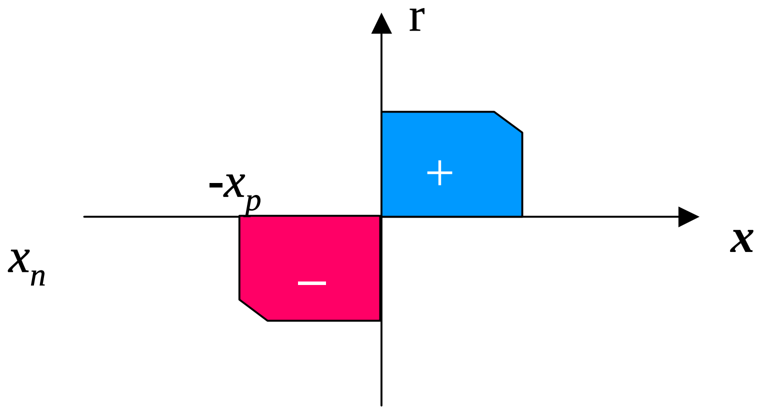
- For a pn junction, electrons and holes will <u>diffuse</u> through the junction, which would result in net r in the space charge region.

P-N Junction


p-type Si, N_A
n-type Si, N_D
Metal contact
Anode
Cathode
Depletion region
Ionized dopants

Charge Distribution in PN Junction

- Net *r* results in the depletion region (or space charge region)
- $\rho = \begin{cases} -qN_A & -x_p \le x \le 0 \\ qN_D & 0 \le x \le x_p \end{cases}$



$$Q\,\frac{dE}{dx} = \frac{r}{k_S e_o} = \frac{q}{k_S e_o}\begin{cases} -N_A & -x_p \le x \le 0 \\ N_D & 0 \le x \le x_n \end{cases}$$

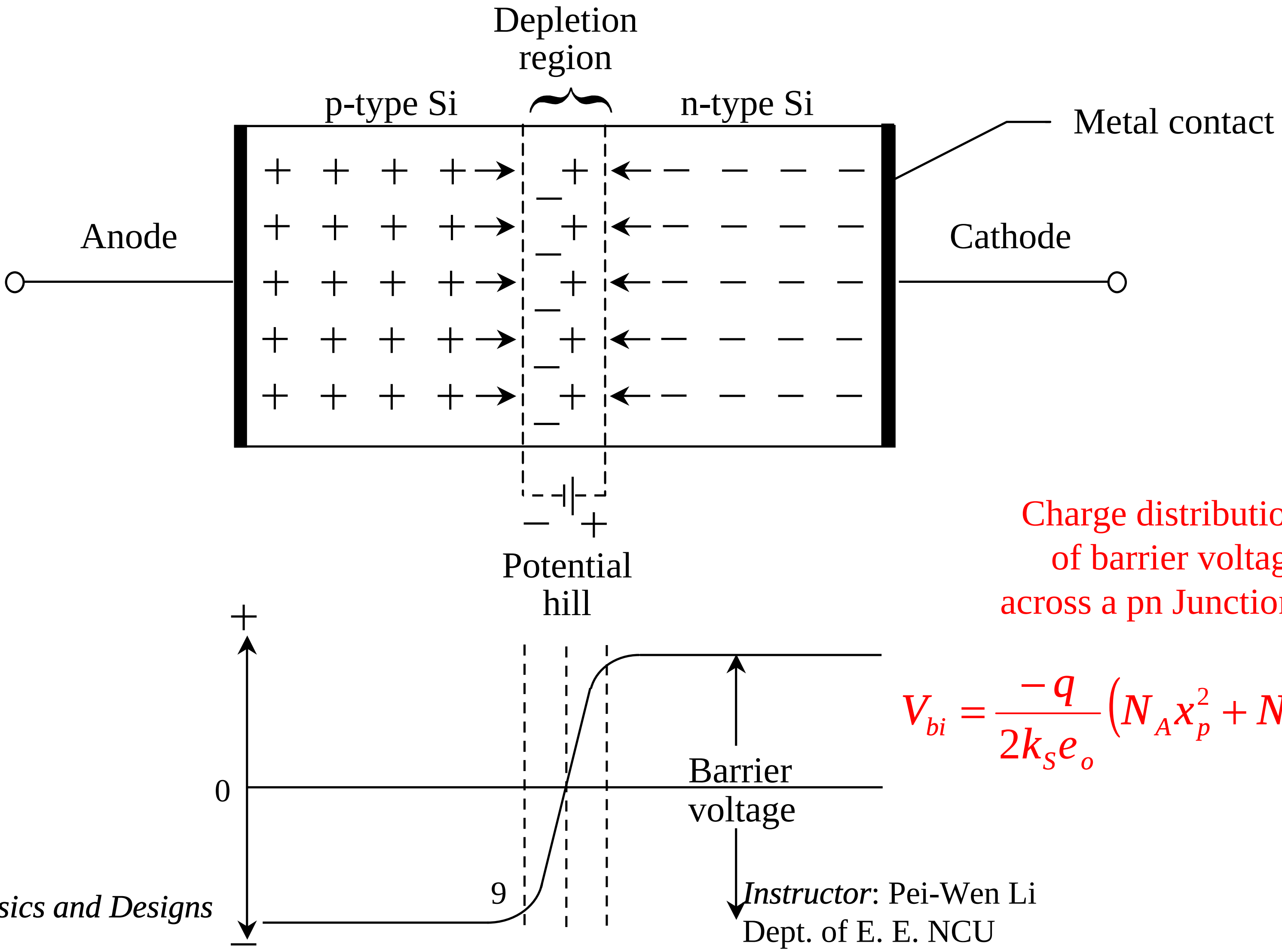
$$\Rightarrow E(x) = \frac{1}{k_S e_o}\int_{x_n}^{x} r(x) + E(x_n), \quad E(x_n) = 0, Q\,\frac{dV}{dx} = 0$$

Charge neutrality

$$\Rightarrow E(x) = -\frac{q}{k_S e_o}(N_A x) - \frac{q}{k_S e_o}N_D x_n \quad \text{if } x < 0$$

$$E(x) = \frac{q}{k_S e_o}(N_D x) - \frac{q}{k_S e_o}N_D x_n \quad \text{if } x > 0 \Rightarrow E(x_n) = 0, E(x_p) = 0 \Rightarrow \boxed{N_A x_p = N_D x_n}$$

Open-Circuit Condition of a pn Junction Diode



Charge distribution of barrier voltage across a pn Junction.

$$V_{bi} = \frac{-q}{2k_S e_o}\left(N_A x_p^2 + N_D x_n^2\right)$$

Width of Space Charge Region

- Recall $x_nN_D = x_pN_A$,

$$\Rightarrow x_n = \left[\frac{2k_s e_o}{q} \frac{N_A}{N_D(N_A + N_D)} V_{bi} \right]^{1/2}$$

$$x_p = \left[\frac{2k_s e_o}{q} \frac{N_D}{N_D(N_A + N_D)} V_{bi} \right]^{1/2}$$

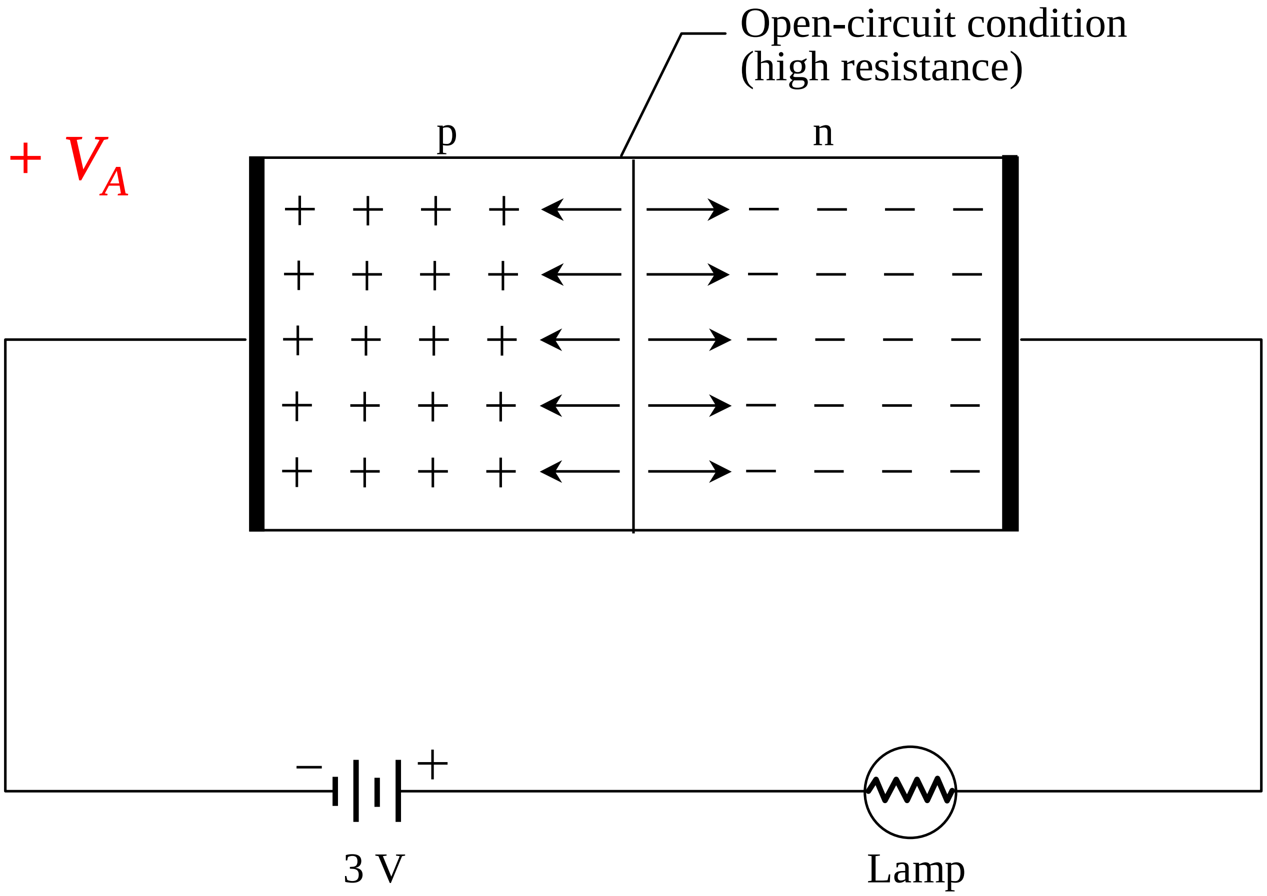
$$\Rightarrow W = x_n + x_p = \frac{2k_s e_o}{q} \left[\frac{N_A N_D}{(N_A + N_D)} V_{bi} \right]^{1/2}$$

- W is dependent on the built-in voltage V_{bi}.

Reverse-Biased PN Junction Diode

$V_{bi} \rightarrow V_{bi} + V_A$

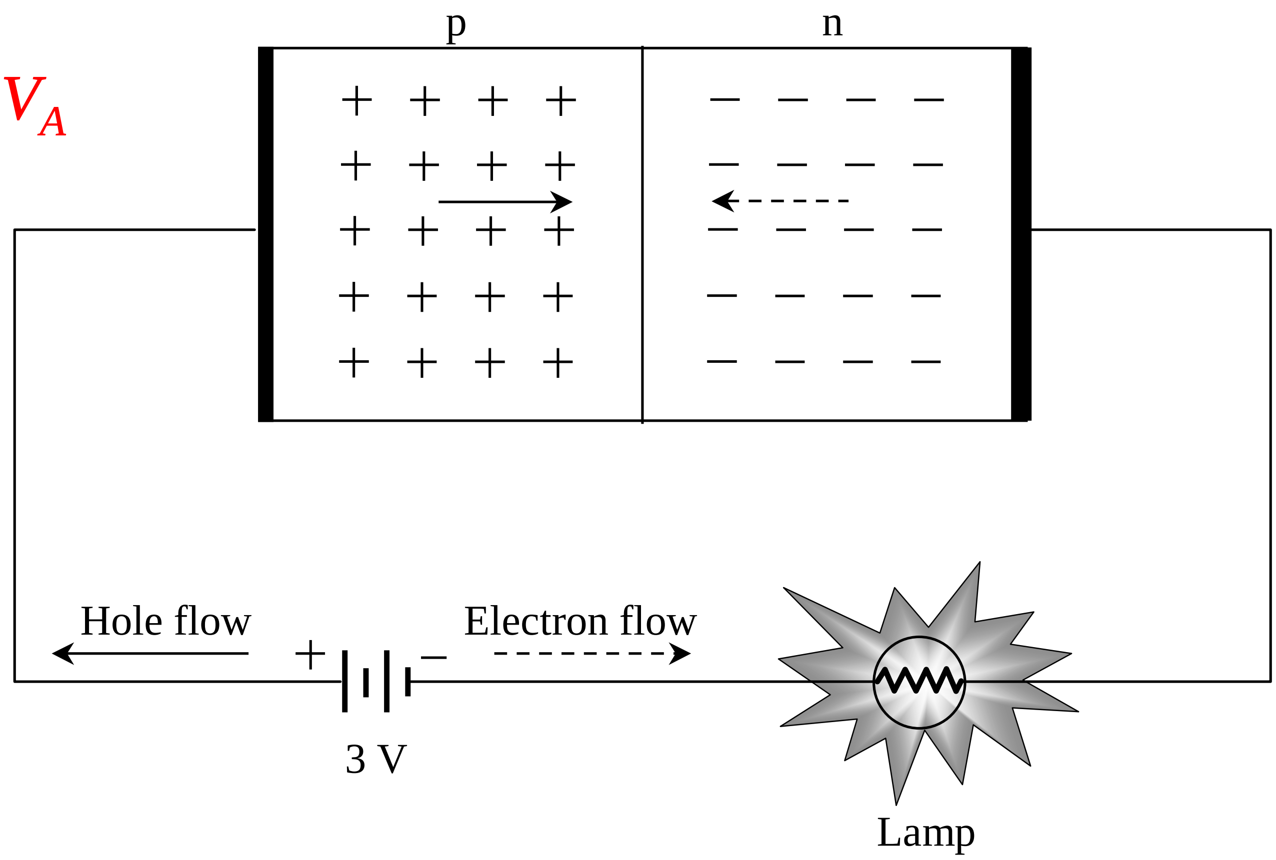
$W \uparrow\uparrow$



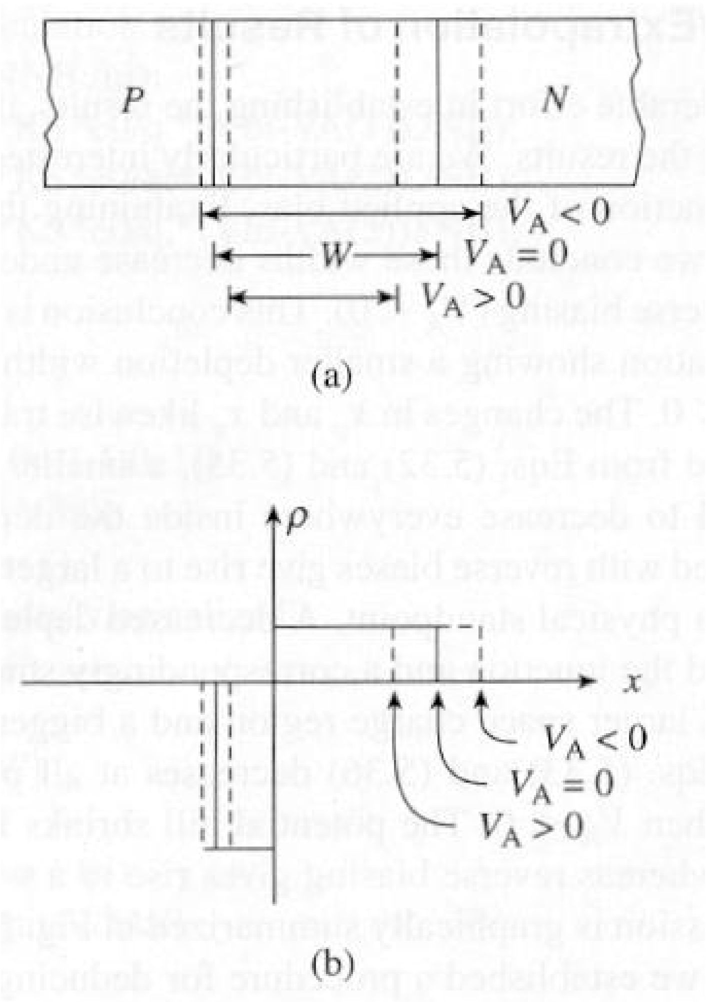
Forward-Biased PN Junction Diode

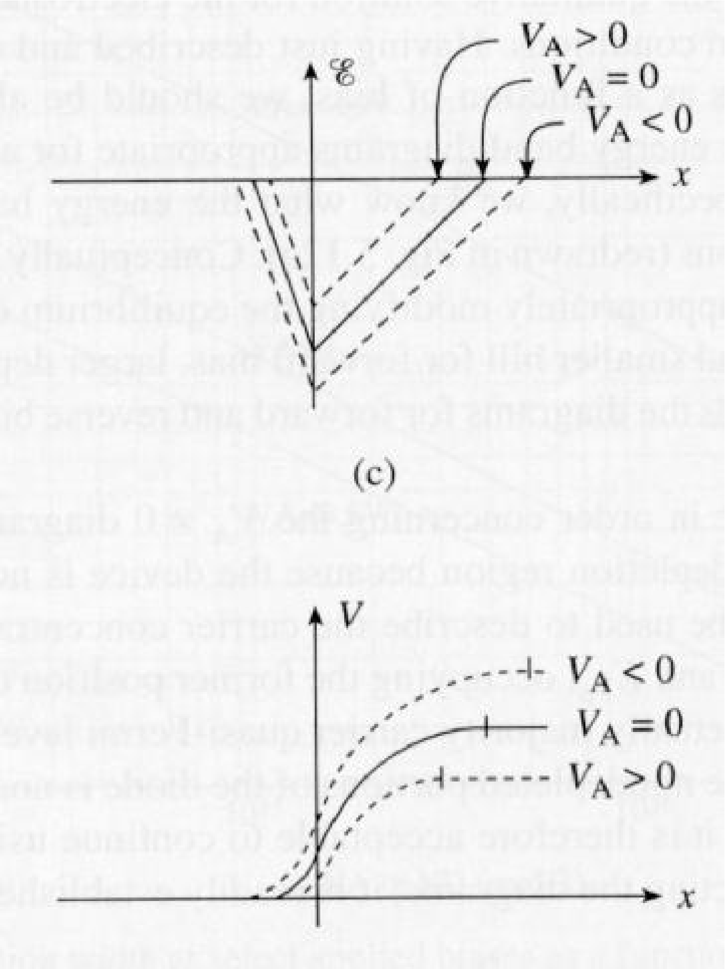
$V_{bi} \rightarrow V_{bi} - V_A$

$W \downarrow \downarrow$



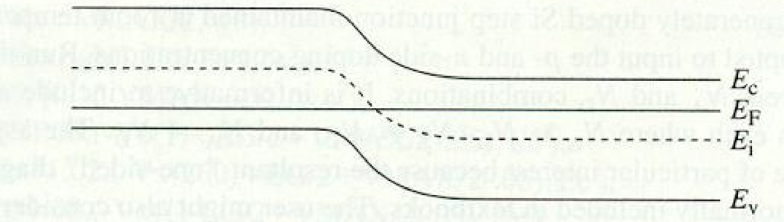
Bias Effect on the PN Junction



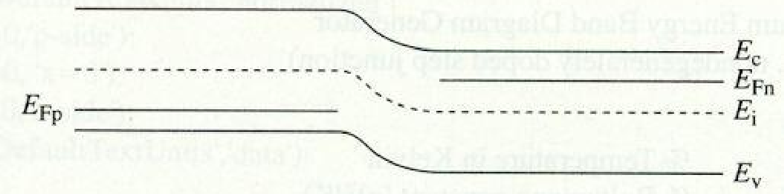


Bias Effect on the PN Junction Band Diagrams

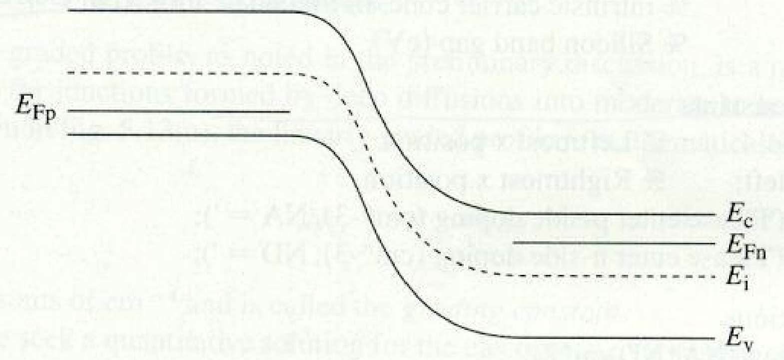
- Fig. 5.12



(a) Equilibrium ($V_A = 0$)



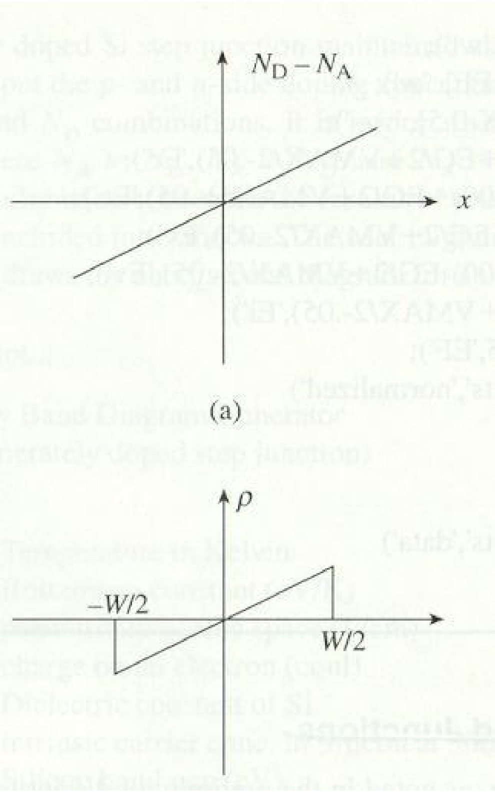
(b) Forward bias ($V_A > 0$)

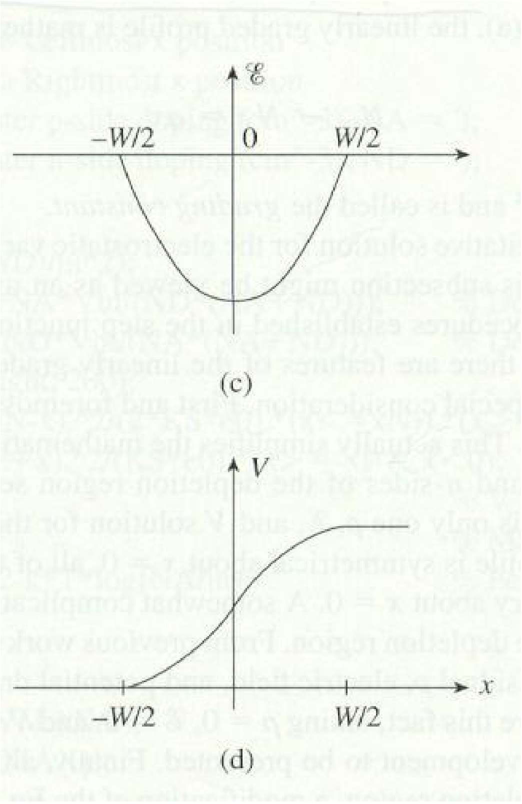


(c) Reverse bias ($V_A < 0$)

Linearly Graded PN Junction

- Assume the linearly graded profile is $N_D - N_A = ax$, *a*: grading const.





$$\Rightarrow W = \left[\frac{12 k_S e_o}{qa} \left(V_{bi} - V_A \right) \right]^{1/3}$$

Continuity Equations

- There will be a change in carrier concentrations within a given small regions of the semiconductor if an imbalance exists between the total currents into and out of the region.

$$q\frac{\partial n}{\partial t} = \nabla \bullet J_N$$

$$q\frac{\partial p}{\partial t} = -\nabla \bullet J_P$$

- Minority Carrier Diffusion Equation

$$\nabla \bullet J_N = \nabla \bullet \left(qD_N \frac{\partial n}{\partial x} \right) = qD_N \frac{\partial^2 n}{\partial x^2} = qD_N \frac{\partial^2 (\Delta n)}{\partial x^2}$$

$$\Rightarrow q\frac{\partial n_P}{\partial t} = qD_N \frac{\partial^2 n_P}{\partial x^2} = qD_N \frac{\partial^2 (\Delta n_P)}{\partial x^2}$$

$$q\frac{\partial p_N}{\partial t} = qD_P \frac{\partial^2 p_N}{\partial x^2} = qD_P \frac{\partial^2 (\Delta p_N)}{\partial x^2}$$

Continuity Equations

- If thermal R-G is considered, continuity equations would be modified

$$\frac{\partial n}{\partial t} = \frac{1}{q}\nabla \bullet J_N + \left.\frac{\partial n}{\partial t}\right|_{\substack{\text{thermal}\\ \text{R-G}}}$$

$$\frac{\partial p}{\partial t} = \frac{-1}{q}\nabla \bullet J_P + \left.\frac{\partial p}{\partial t}\right|_{\substack{\text{thermal}\\ \text{R-G}}} \qquad \left.\frac{\partial n}{\partial t}\right|_{\substack{\text{thermal}\\ \text{R-G}}} = -\frac{\Delta n}{t_n},\ t_n : \text{time const.}$$

- ⇒Minority carrier Diffusion equations become

$$\frac{\partial n_P}{\partial t} = D_N \frac{\partial^2 (\Delta n_P)}{\partial x^2} - \frac{\Delta n_P}{t_n}$$

$$\frac{\partial p_N}{\partial t} = D_P \frac{\partial^2 (\Delta p_N)}{\partial x^2} - \frac{\Delta p_n}{t_p}$$

Diffusion Length

- The average distance minority carriers can diffuse into a sea of majority carriers before being annihilated.

$$L_P \equiv \sqrt{D_P \tau_p} \text{ --- minority carrier holes in an n-type material}$$

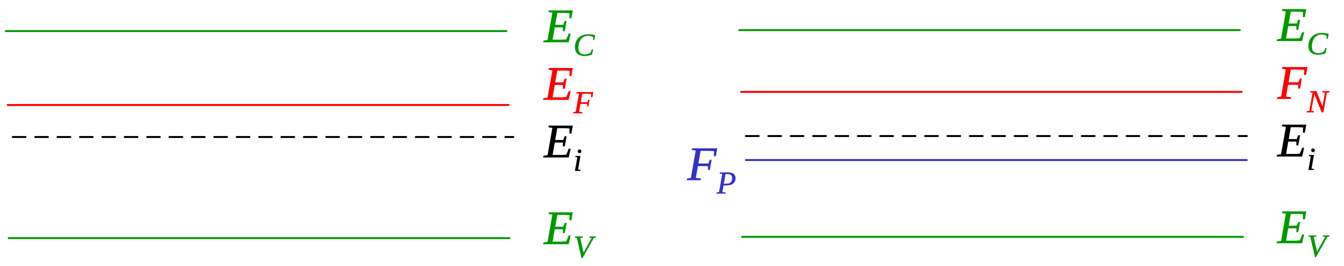
$$L_N \equiv \sqrt{D_N \tau_n} \text{ --- minority carrier electrons in a p-type material}$$

Quasi-Fermi levels

- Are energy levels used to specify the carrier concentrations inside a semiconductor under nonequilibrium conditions.

$$n \equiv n_i e^{\left(E_{F_N}-E_i\right)/kT} \quad \text{or} \quad F_N \equiv E_i + kT\ln\left(\frac{n}{n_i}\right)\text{: quasi - fermi level for electrons under nonequilibrium cases}$$

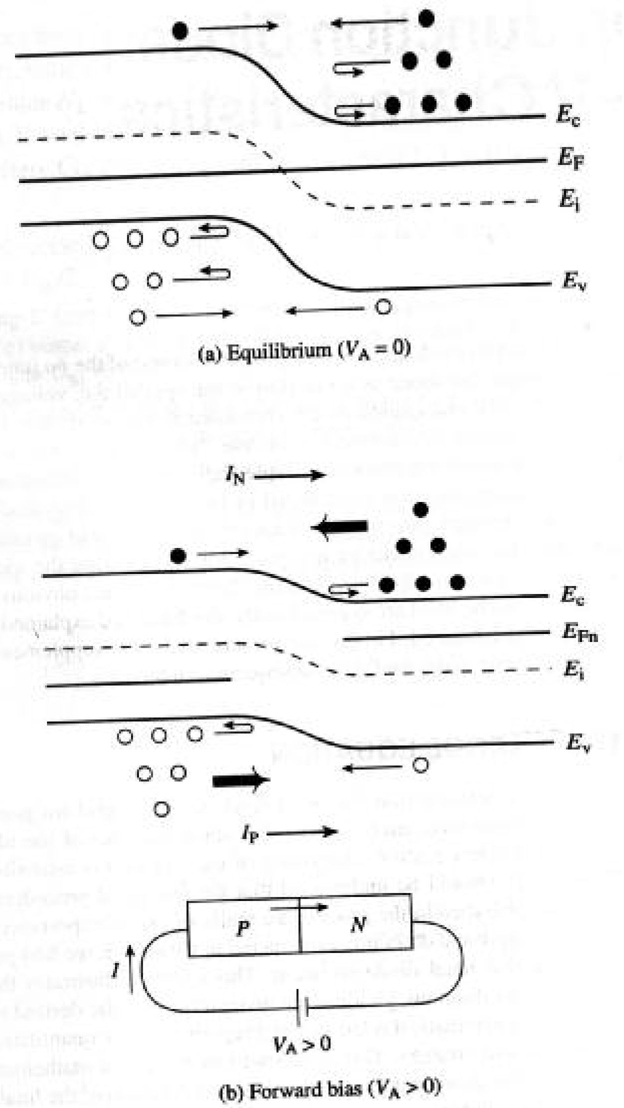
$$p \equiv n_i e^{\left(E_i-E_{F_P}\right)/kT} \quad \text{or} \quad F_P \equiv E_i - kT\ln\left(\frac{p}{n_i}\right)\text{: quasi - fermi level for holes under nonequilibrium cases}$$



Under equilibrium

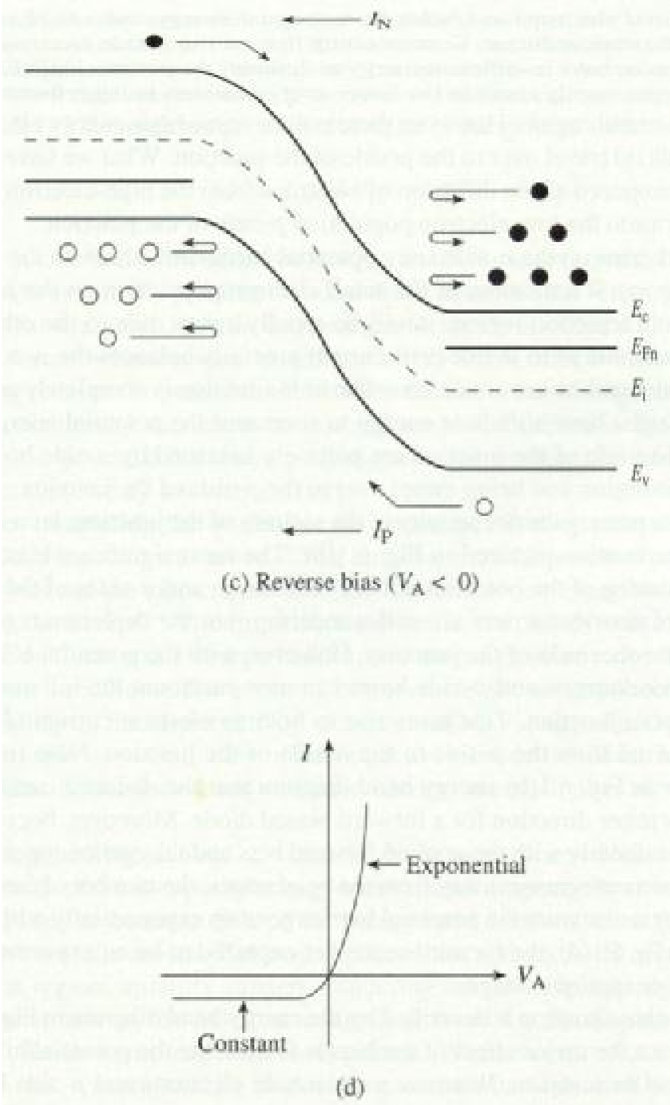
Under non-equilibrium

PN Diodes: I-V Characteristics



(a) Equilibrium ($V_A = 0$)

(b) Forward bias ($V_A > 0$)

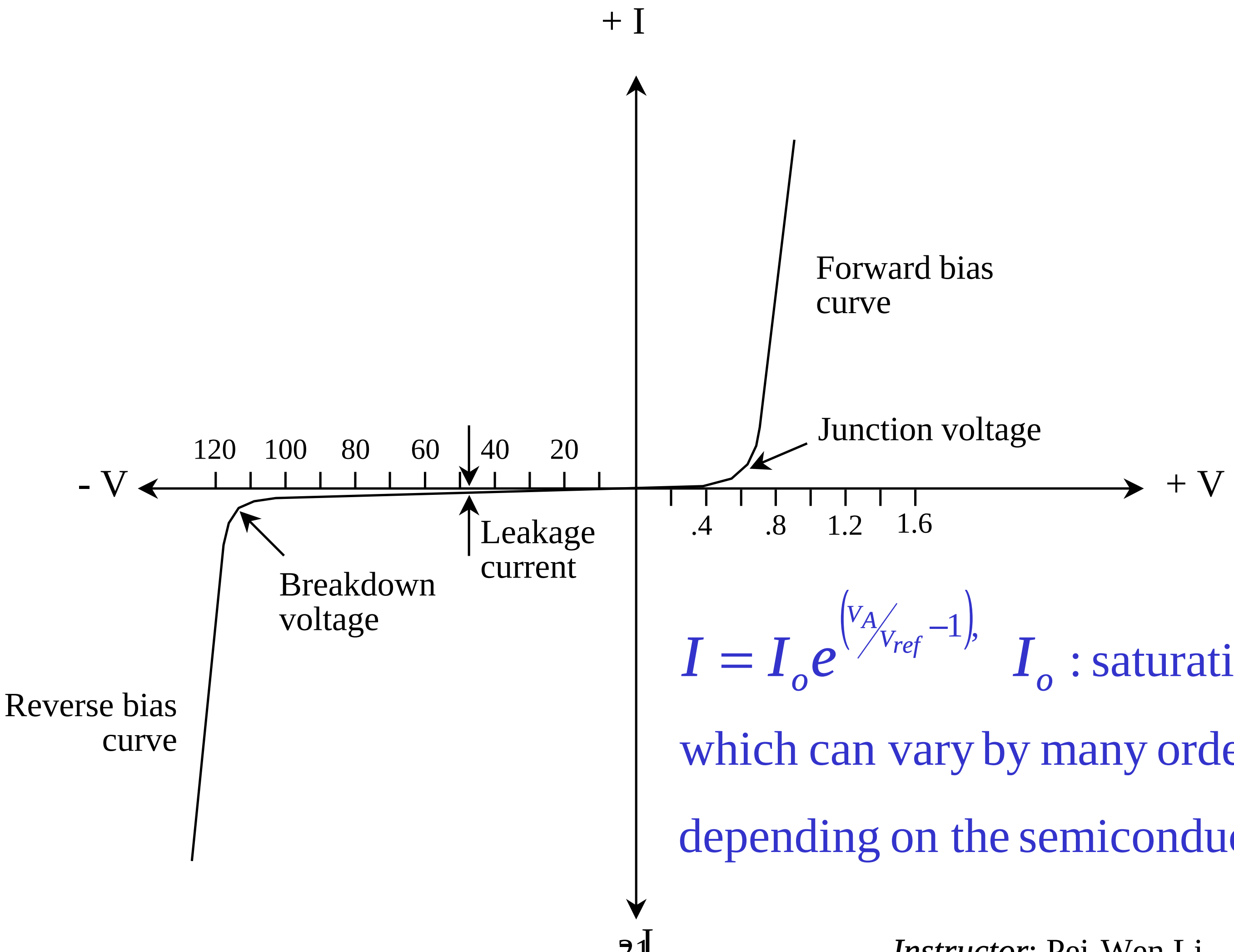


(c) Reverse bias ($V_A < 0$)

(d)

Figure 6.1 *Continued.*

Forward and Reverse Electrical Characteristics of a Silicon Diode



$I = I_o e^{\left(V_A / V_{ref} - 1\right)}$, I_o : saturation current, which can vary by many orders of magnitude depending on the semiconductors

Composite energy-band/circuit diagram of a reverse-biased pn diode

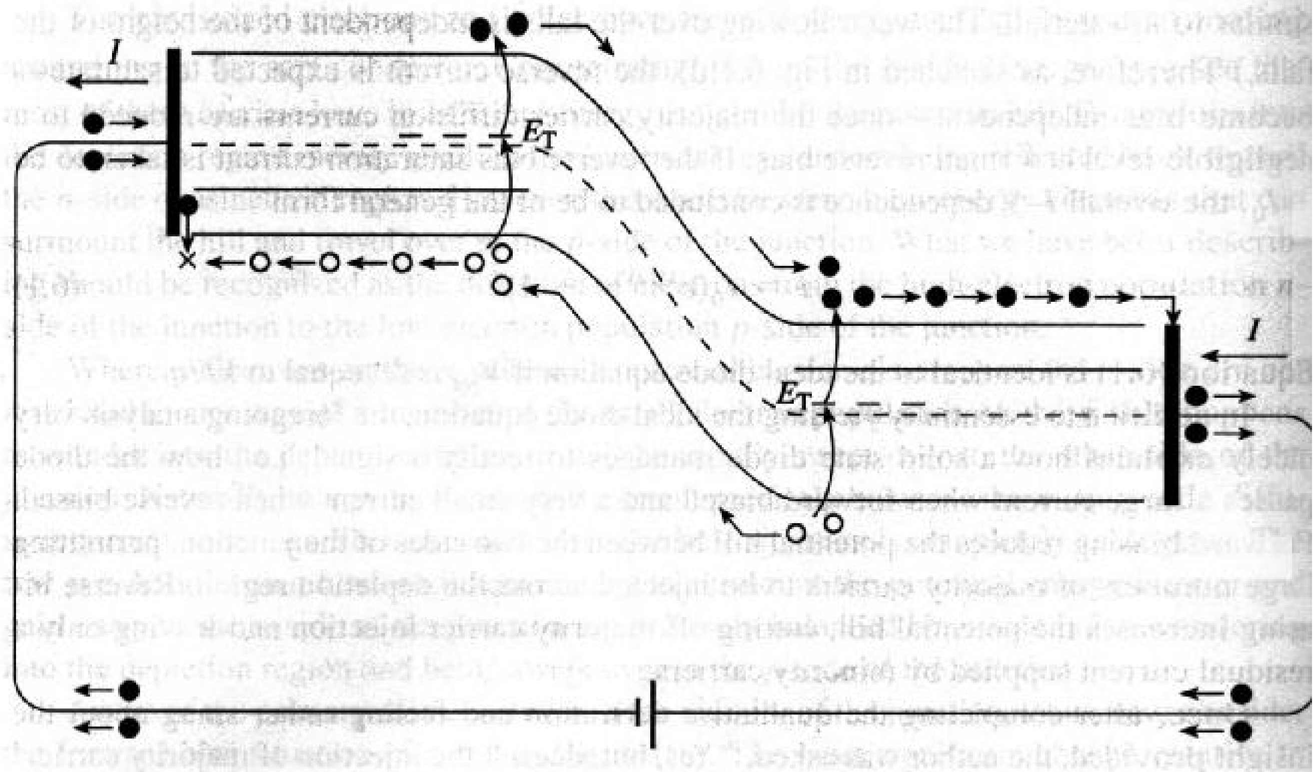


Figure 6.2 Composite energy-band/circuit diagram providing an overall view of carrier activity inside a reverse-biased *pn* junction diode. The capacitor-like plates at the outer ends of the energy band diagram schematically represent the ohmic contacts to the diode.

I-V Characteristics

- From deviation:

$$I_o = qA\left(\frac{D_N}{L_N}\frac{n_i^2}{N_A} + \frac{D_P}{L_P}\frac{n_i^2}{N_D}\right)$$

- So for p$^+$/n diode,

$$N_A >> N_D \Rightarrow I_o \cong qA\frac{D_P}{L_P}\frac{n_i^2}{N_D}$$

- For n$^+$/p diode,

$$N_D >> N_A \Rightarrow I_o \cong qA\frac{D_N}{L_N}\frac{n_i^2}{N_A}$$

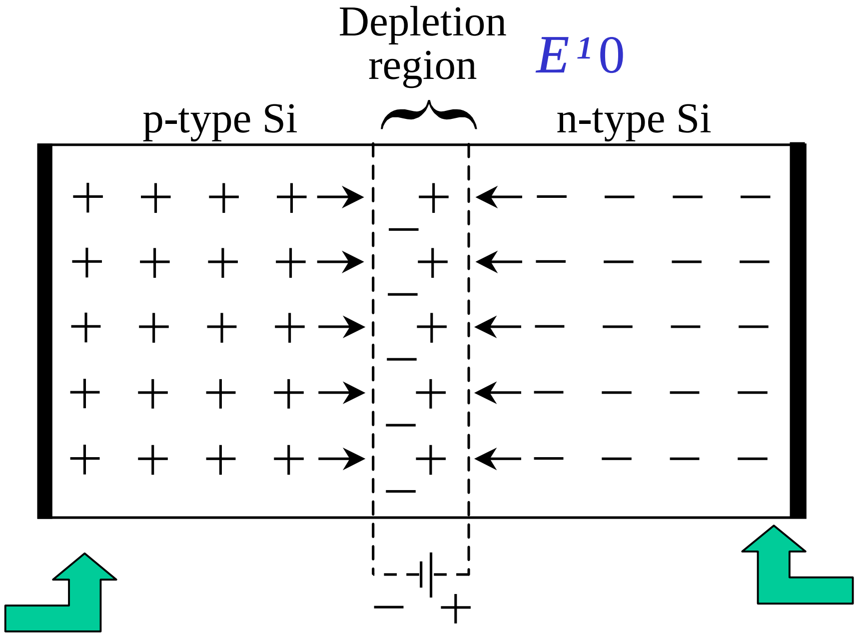
- As a general rule, this suggests that the heavily doped side of an asymmetrical junction can be ignored in determining the electrical characteristics of the junction.

Derivation of I-V Characteristics

$$J = J_N(x) + J_P(x)$$

$$J_N = q\mu_n nE + qD_N \frac{dn}{dx}$$

$$J_P = q\mu_p pE - qD_P \frac{dp}{dx}$$



Quasi-neutral p region

$E \sim 0$

Quasi-neutral n region

$E \sim 0$

Derivation of I-V Characteristics

- In quasi-neutral regions, E = 0, so consider diffusion and thermal R-G currents only.

$$J_N = qD_N \frac{d\Delta n_p}{dx} \text{ for } x \le -x_p, \frac{\partial n}{\partial t} = D_N \frac{d^2 \Delta n_p}{dx^2} - \frac{\Delta n_p}{t_n} = 0$$

$$J_P = -qD_P \frac{d\Delta p_n}{dx} \text{ for } x \ge x_n, \frac{\partial p}{\partial t} = D_P \frac{d^2 \Delta p_n}{dx^2} - \frac{\Delta p_n}{t_n} = 0$$

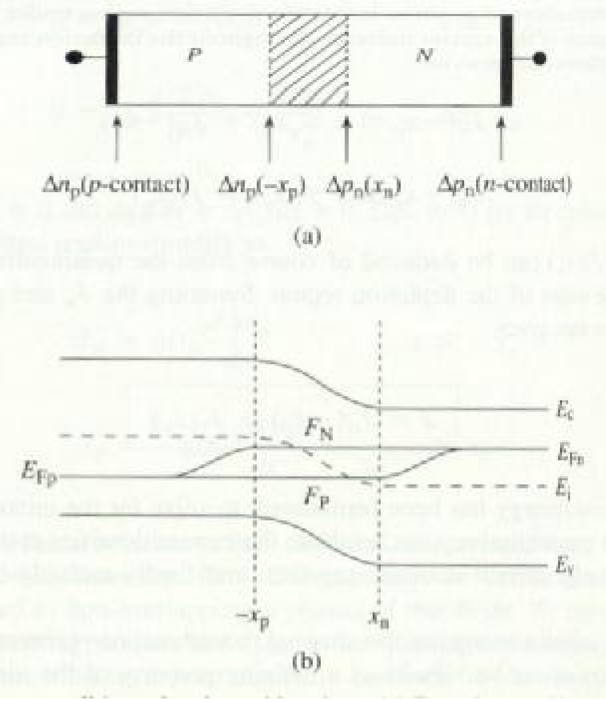
- In Depletion Region:

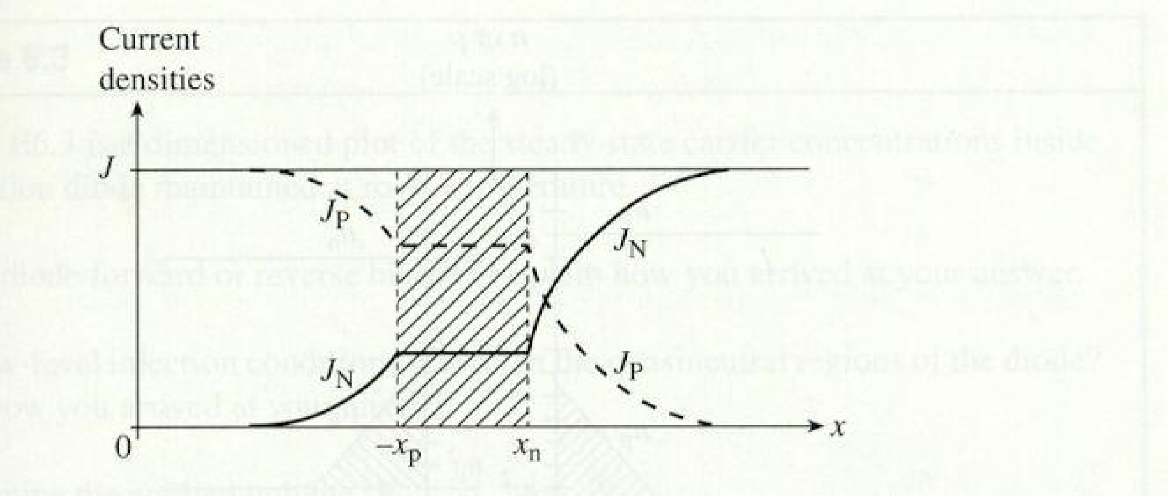
$$0 = \frac{\partial n}{\partial t} = \frac{1}{q} \nabla \bullet J_N + \frac{\Delta n_p}{t_n}\bigg|_{\text{thermal}} \Rightarrow \frac{dJ_N}{dx} = 0 \Rightarrow J_N = \text{const.} = J_N(-x_p)$$

$$\text{similarily, } J_P = \text{const.} = J_P(x_n)$$

$$J = J_N + J_P$$

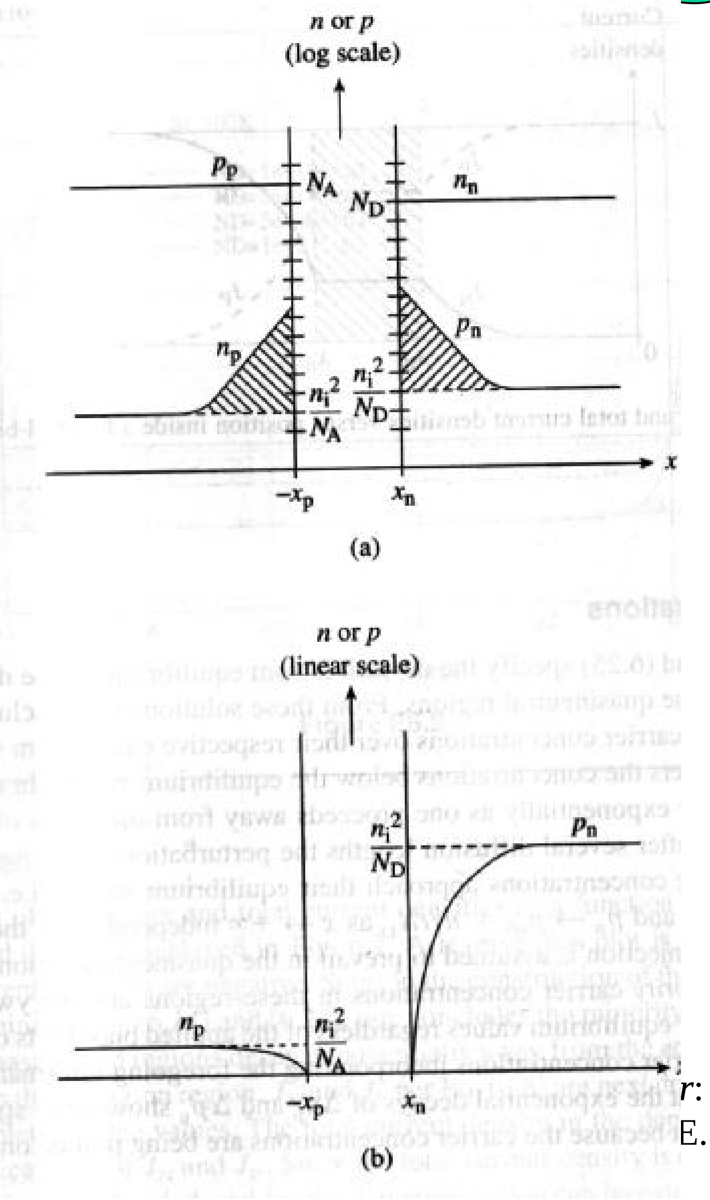
Boundary conditions and quasi fermi level inside a forward-biased diode



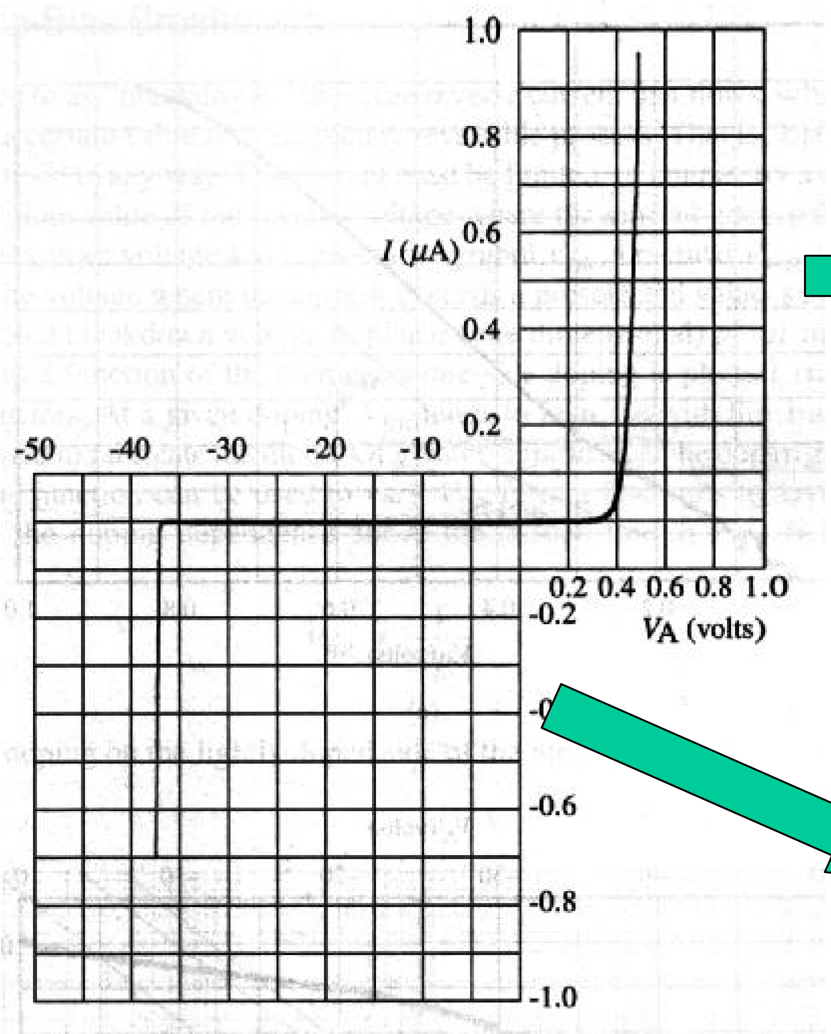


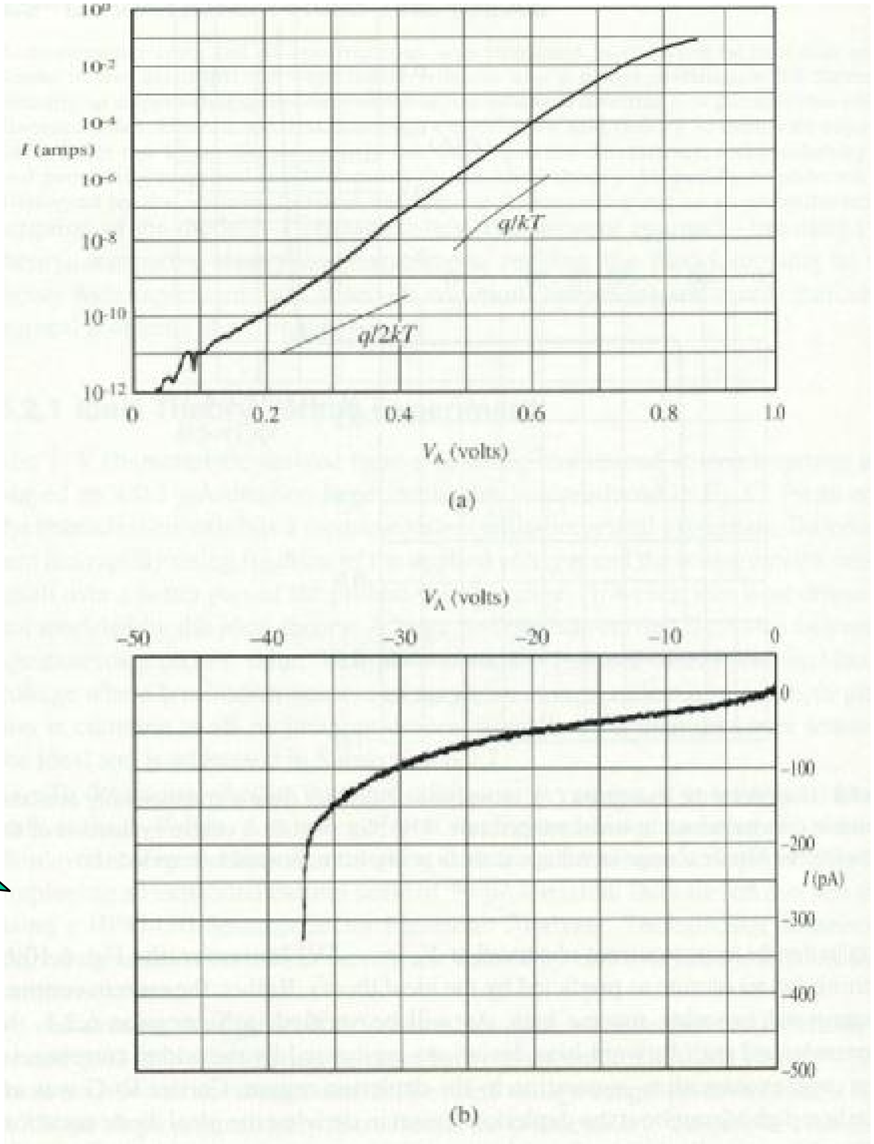
Carrier and total current densities versus position inside a forward-biased *pn* junction

Carrier Concentration inside a pn diode under forward and reverse biasing.



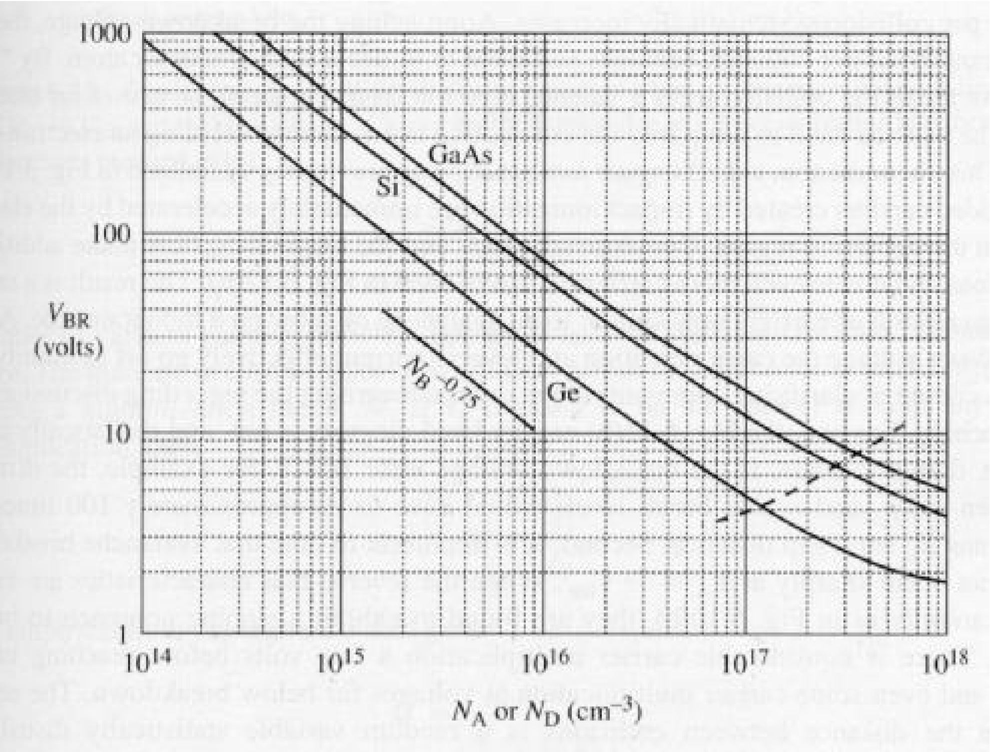
Experimental I-V Characteristics





Reverse-Bias Breakdown

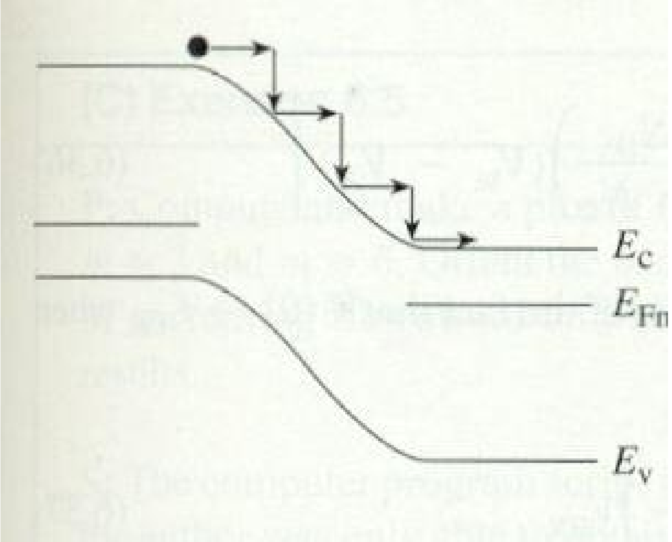
- Large reverse current flows when the reverse voltage exceeds a certain value, V_{BR}. The current must be limited to avoid excessive "heating".
- Practical V_{BR} measurements typically quote the voltage where the reverse current exceeds 1 μA.
- Factors to affect V_{BR}: $V_{BR} \propto \frac{1}{N_B^{0.75}}$
  - 1. Bandgap of the semiconductor.
  - 2. doping on the lightly doped side of the pn junction, N_B.



- Breakdown Mechanism:
  - Avalanche process
  - Zener process

Avalanching

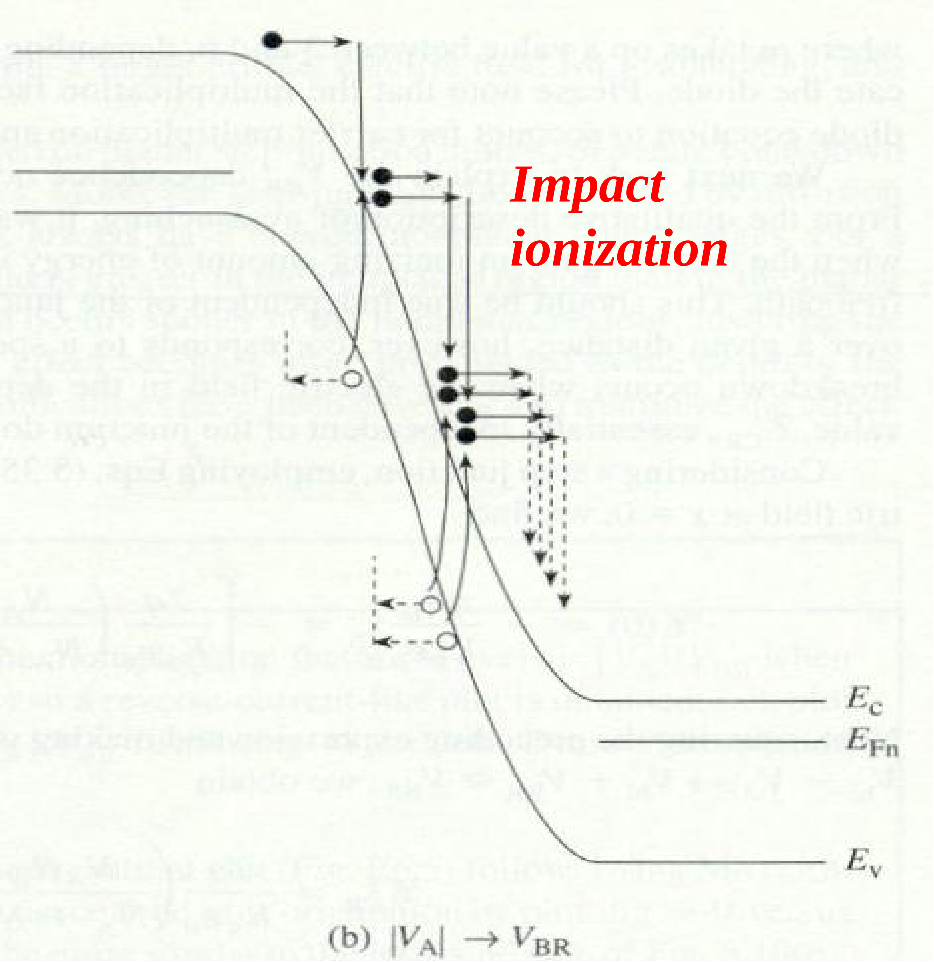
- **As $V_A << V_{BR}$, the reverse current is due to minority carriers randomly entering the depletion region and being accelerated by the E-field.**
- **The acceleration is not continuous but is interrupted by energy-losing collisions with the semiconductor lattice.**
- **Since the mean free path between the collisions is ~10-6 cm, and a median depletion width is ~10-4 cm, a carrier can undergo 10-1000 collisions in crossing the depletion region.**
- **The energy lost by the carrier per collision is small.**
- **The energy transferred to the lattice simply causes lattice vibration --- local heating.**



(a) Small reverse bias

Avalanching

- As V_A ® V_{BR}, the amount of energy transfer to the lattice per collision increases dramatically, and becomes sufficient to ionize a semiconductor atom. That is to causes an electron from the valence band to jump to conduction band. Þ "*impact ionization*"
- The electrons created by impact ioization are immediately accelerated by the large E-field in the depletion region, and consequently, they make additional collisions and create even more energetic electrons. Þ "*Avalanching*"



(b) $|V_A| \to V_{BR}$

Zener Process

- The occurrence of “tunneling” in a reverse-biased diode.
- Two major requirements for tunneling to occur and be significant:
  - There must be filled states on one side of the barrier and empty states on the other side of the barrier at the same energy.
  - The width of the potential energy barrier must be very thin (< 10 nm).
  - That is the doping on the “lightly” doped Si is in excess of 10^{17} cm^{-3}.
  - Zener process is only important in diodes that are heavily doped on both sides.

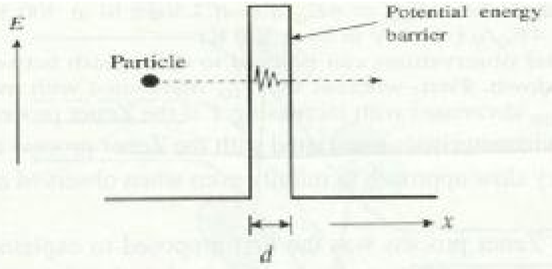


Figure 6.13 General visualization of tunneling.

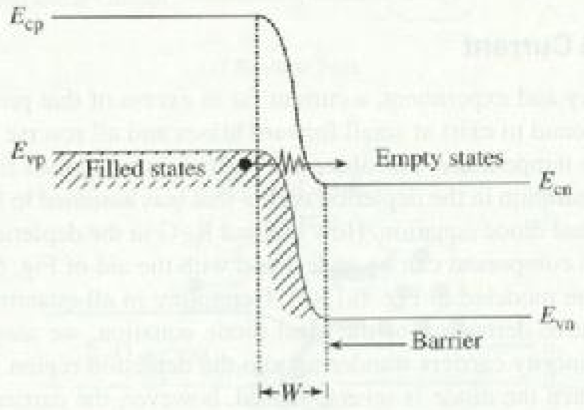
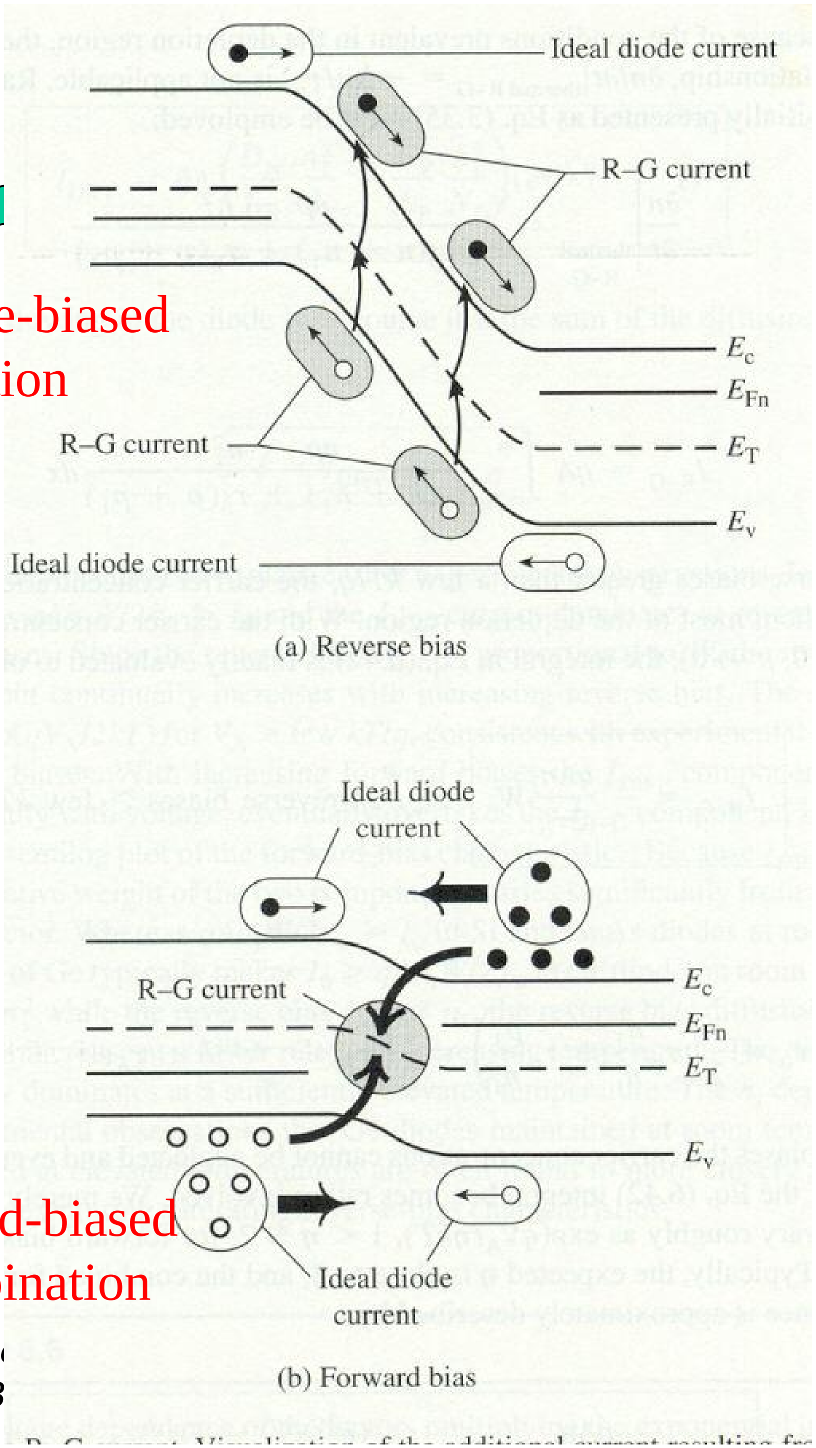


Figure 6.14 Visualization of tunneling in a reverse-biased *pn* junction diode.

R-G Current

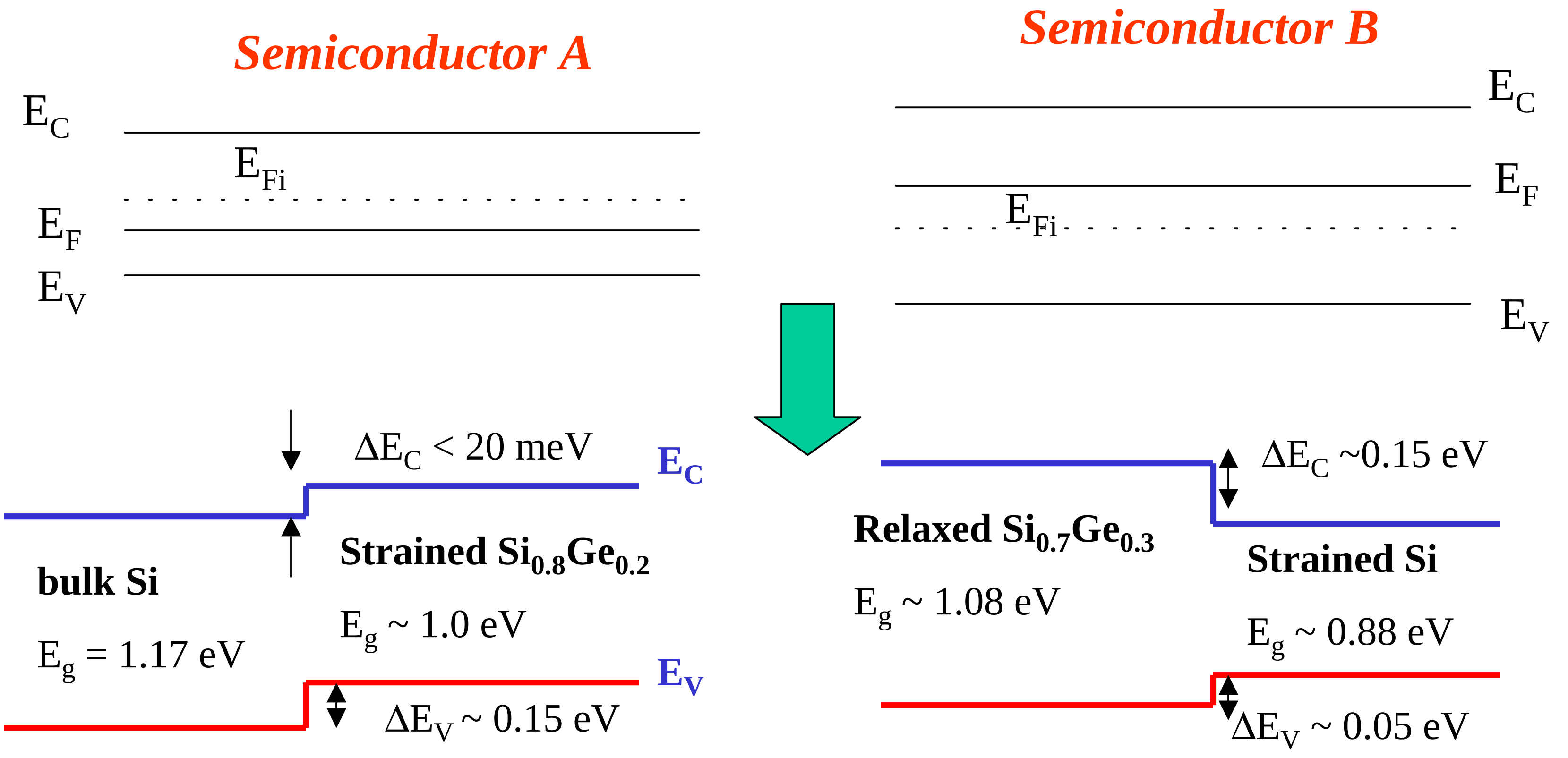
Reverse-biased generation



Forward-biased recombination

- When diode is reverse biased, the carrier concentrations in the depletion region are reduced below their equilibrium values, leading to the thermal generation of electrons and holes throughout the region.
- The large E-field in the depletion region rapidly sweeps the generated carriers onto the quasi-neutral regions, thereby adding to the reverse current.

Hetero-Junction



Semiconductor A

E_C

E_{Fi}

E_F

E_V

Semiconductor B

E_C

E_F

E_{Fi}

E_V

$\Delta E_C < 20$ meV

E_C

bulk Si

$E_g = 1.17$ eV

Strained $Si_{0.8}Ge_{0.2}$

$E_g \sim 1.0$ eV

E_V

$\Delta E_V \sim 0.15$ eV

$\Delta E_C \sim 0.15$ eV

Relaxed $Si_{0.7}Ge_{0.3}$

$E_g \sim 1.08$ eV

Strained Si

$E_g \sim 0.88$ eV

$\Delta E_V \sim 0.05$ eV

Type I Alignment

Type II Alignment

Quantum Well