

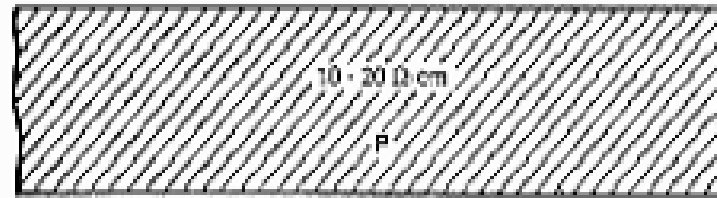
The slide features a decorative layout with blue lines. A vertical line on the left and a horizontal line at the top intersect at a small circle in the top-left corner. Another horizontal line is positioned below the main title. A vertical line on the right and a horizontal line at the bottom intersect at a small circle in the bottom-right corner.

IC製程技術導論(III)

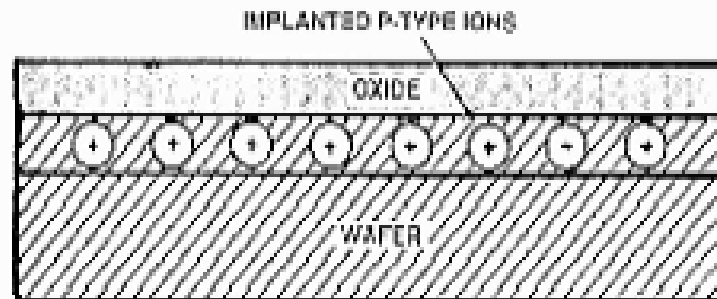
IC製程技術導論(III)

- ☒ NMOS Process Flow及
CMOS Process Flow介紹
- ☒ 教學成效評鑑

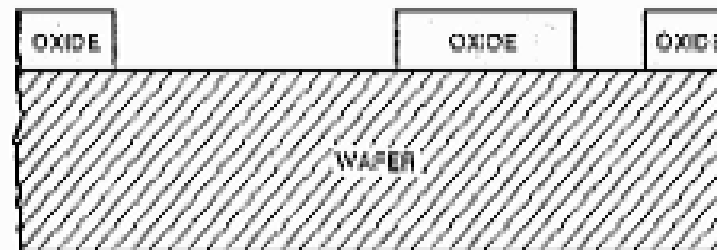
NMOS Process Flow



1. STARTING WAFERS

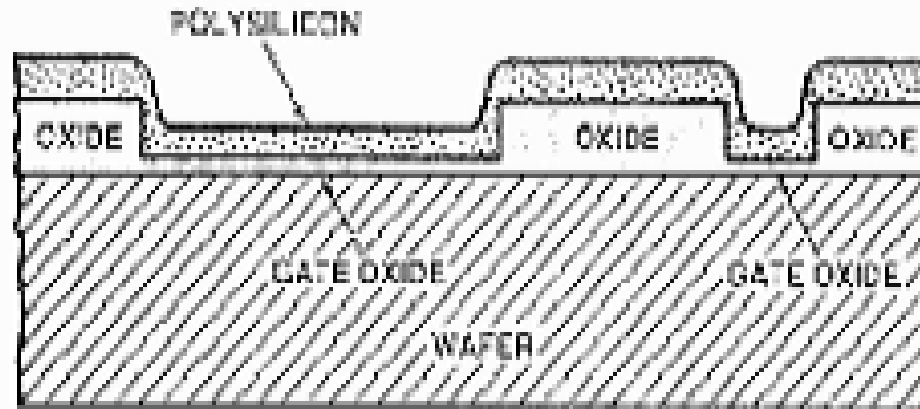


2. THRESHOLD IMPLANT AND INITIAL OXIDE GROWTH

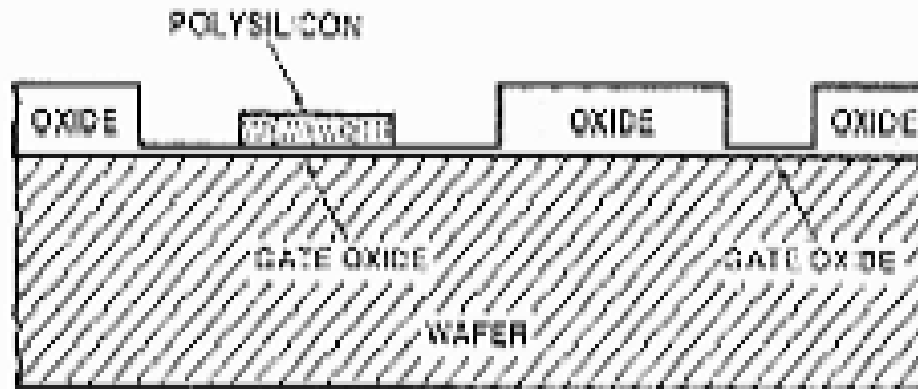


3. ACTIVE AREA PHOTOLITHOGRAPHY

NMOS Process Flow

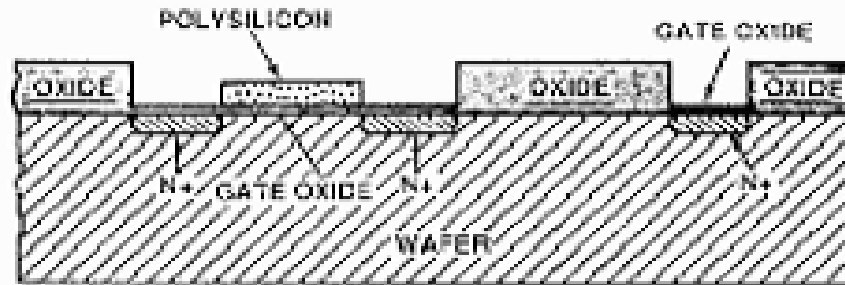


4. GATE OXIDATION AND POLYSILICON DEPOSITION



5. GATE PHOTOLITHOGRAPHY

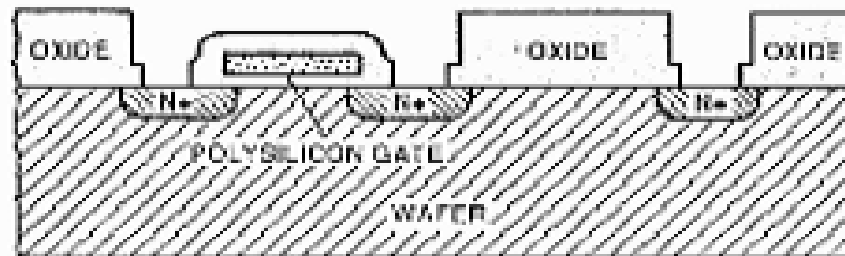
NMOS Process Flow



6. SOURCE/DRAIN IMPLANT

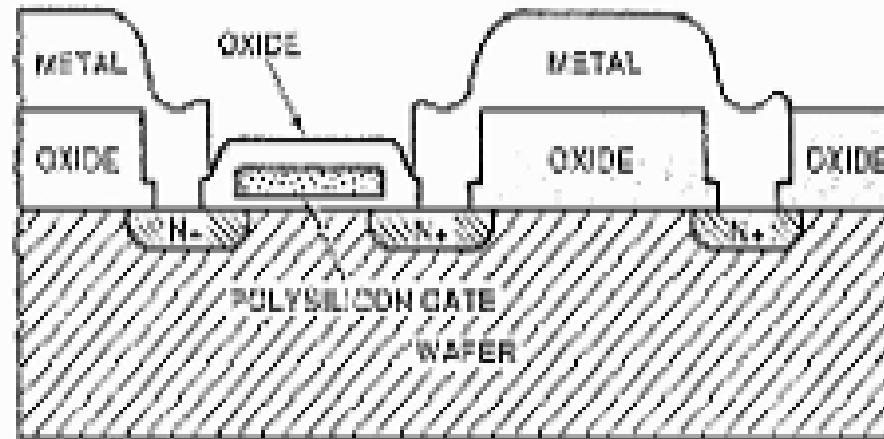


7. SOURCE/DRAIN ANNEAL

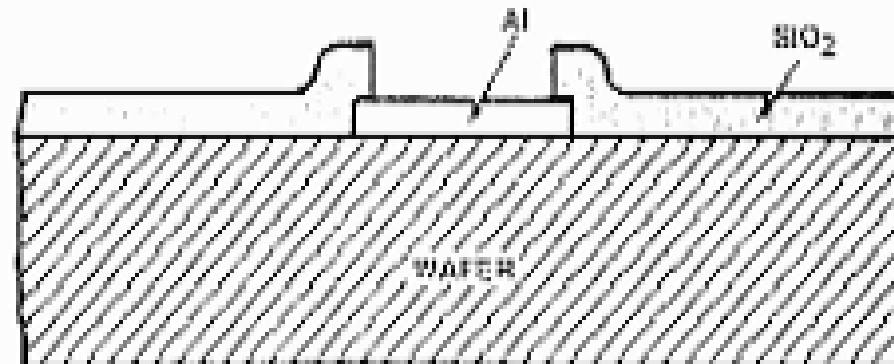


8. CONTACT PHOTOLITHOGRAPHY

NMOS Process Flow

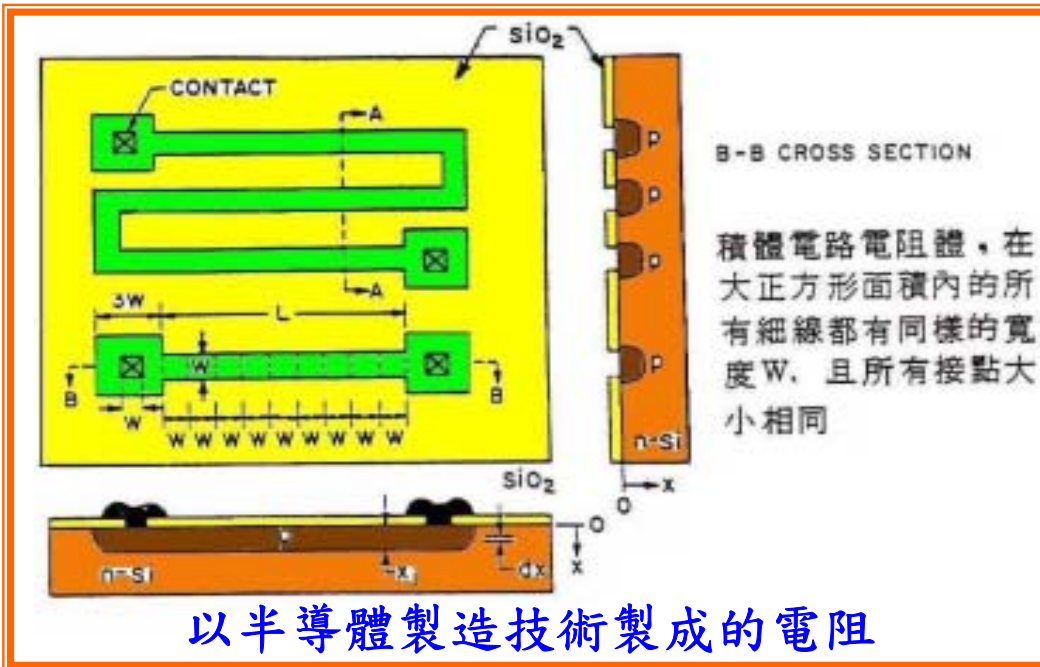


9. METAL DEPOSITION AND PATTERNING

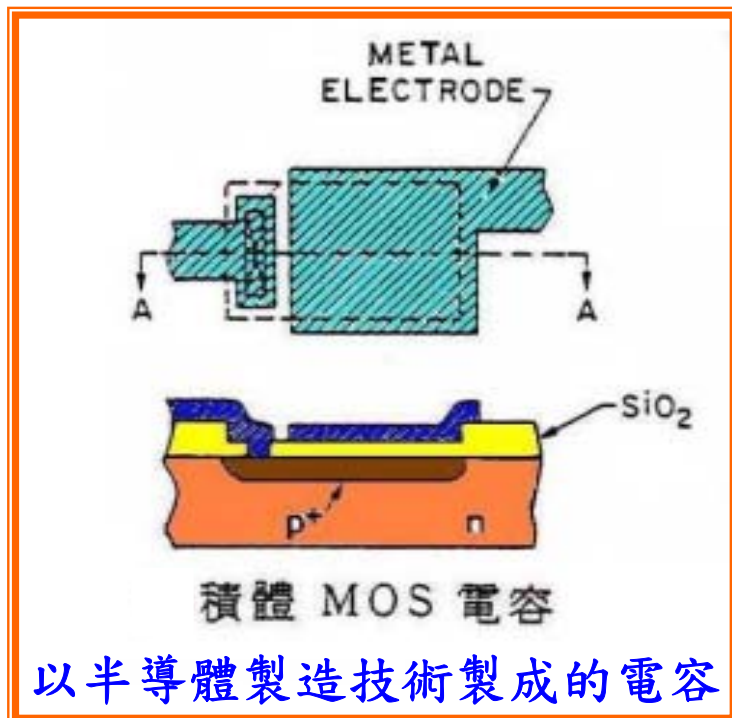


10. REMOVAL OF PASSIVATION FROM BONDING PADS

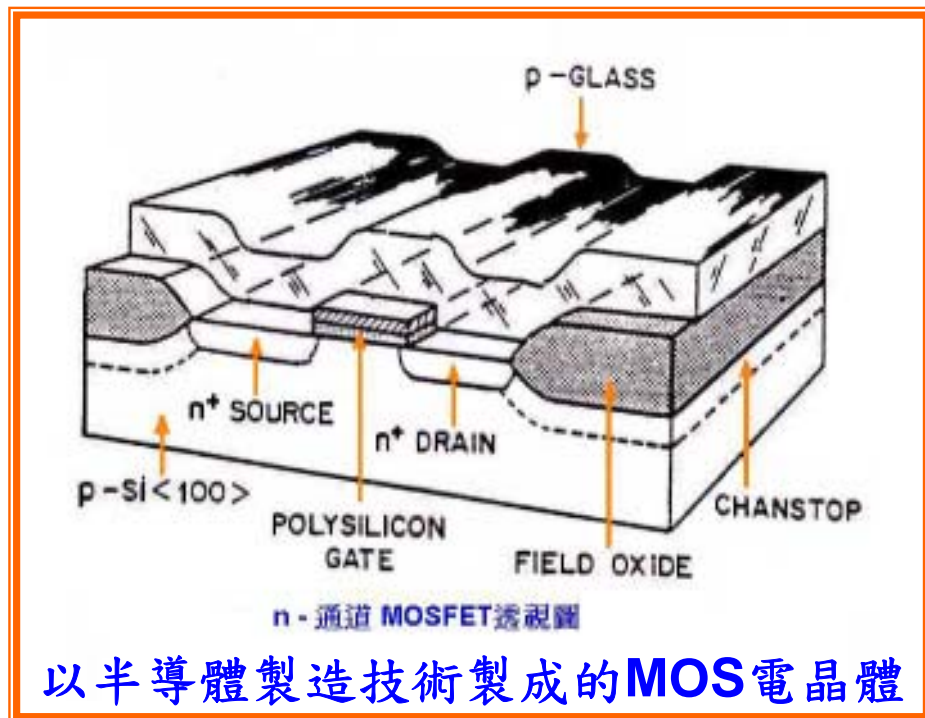
9824A



以半導體製造技術製成的電阻



以半導體製造技術製成的電容



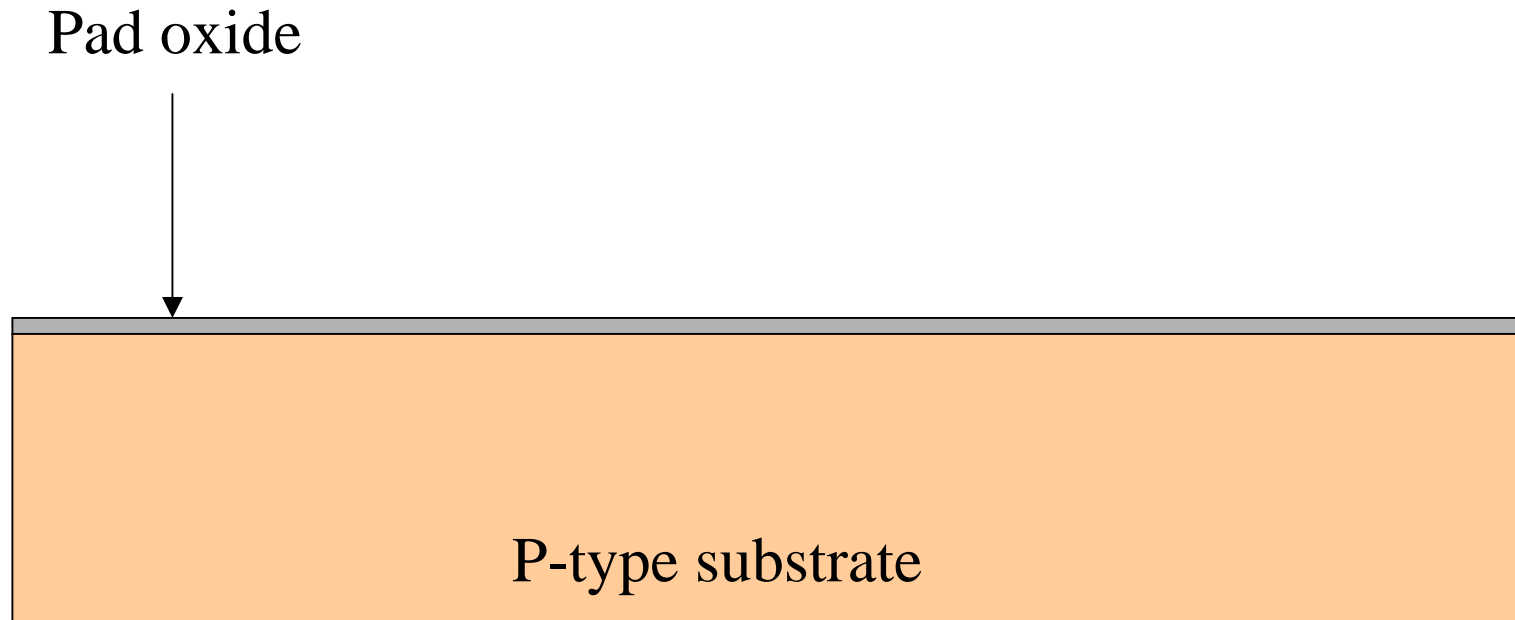
以半導體製造技術製成的MOS電晶體

1 μ m CMOS PROCESS FLOW

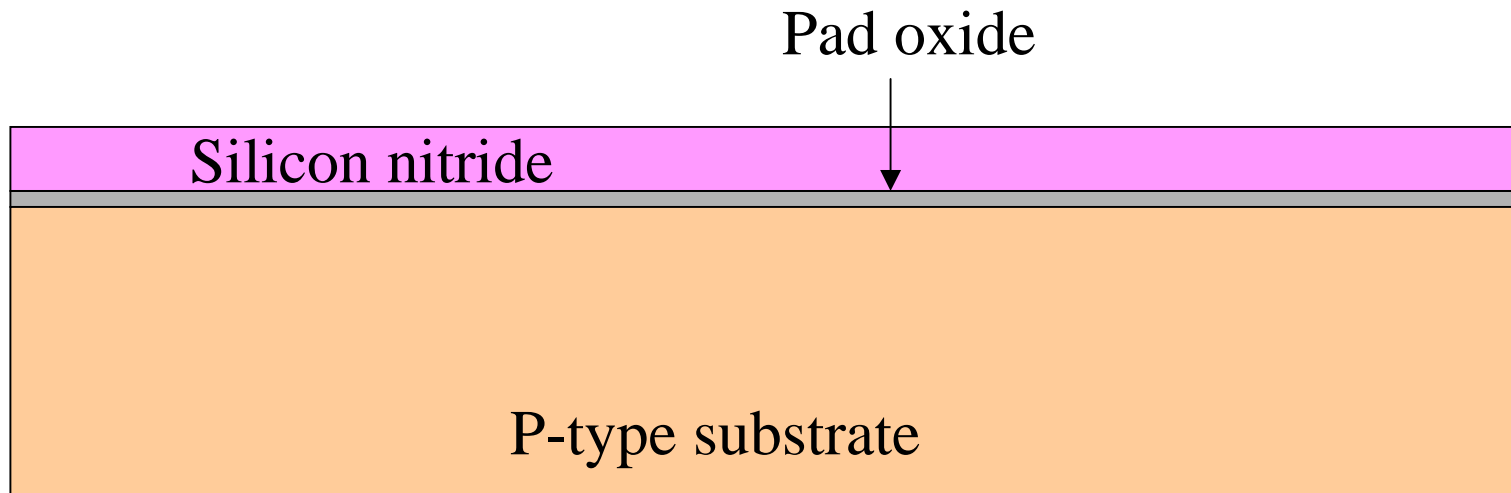
Wafer Clean

P-type substrate

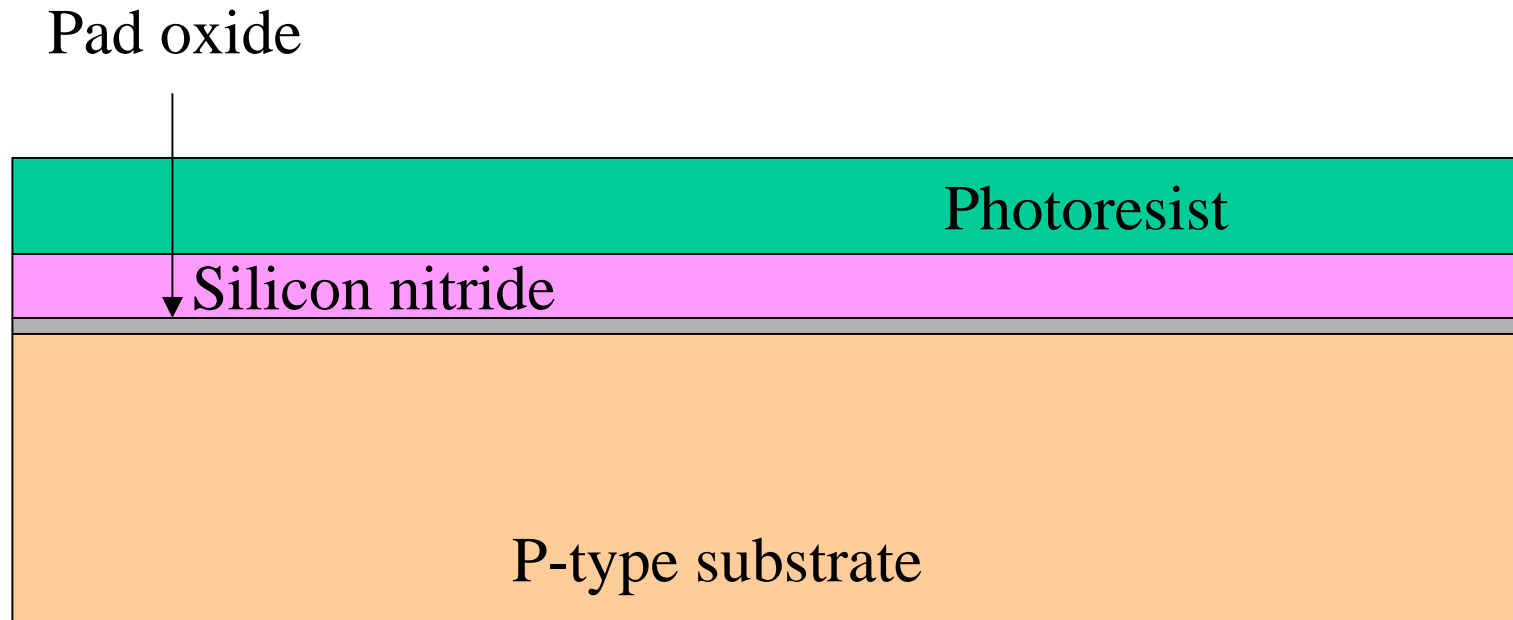
Pad Oxidation



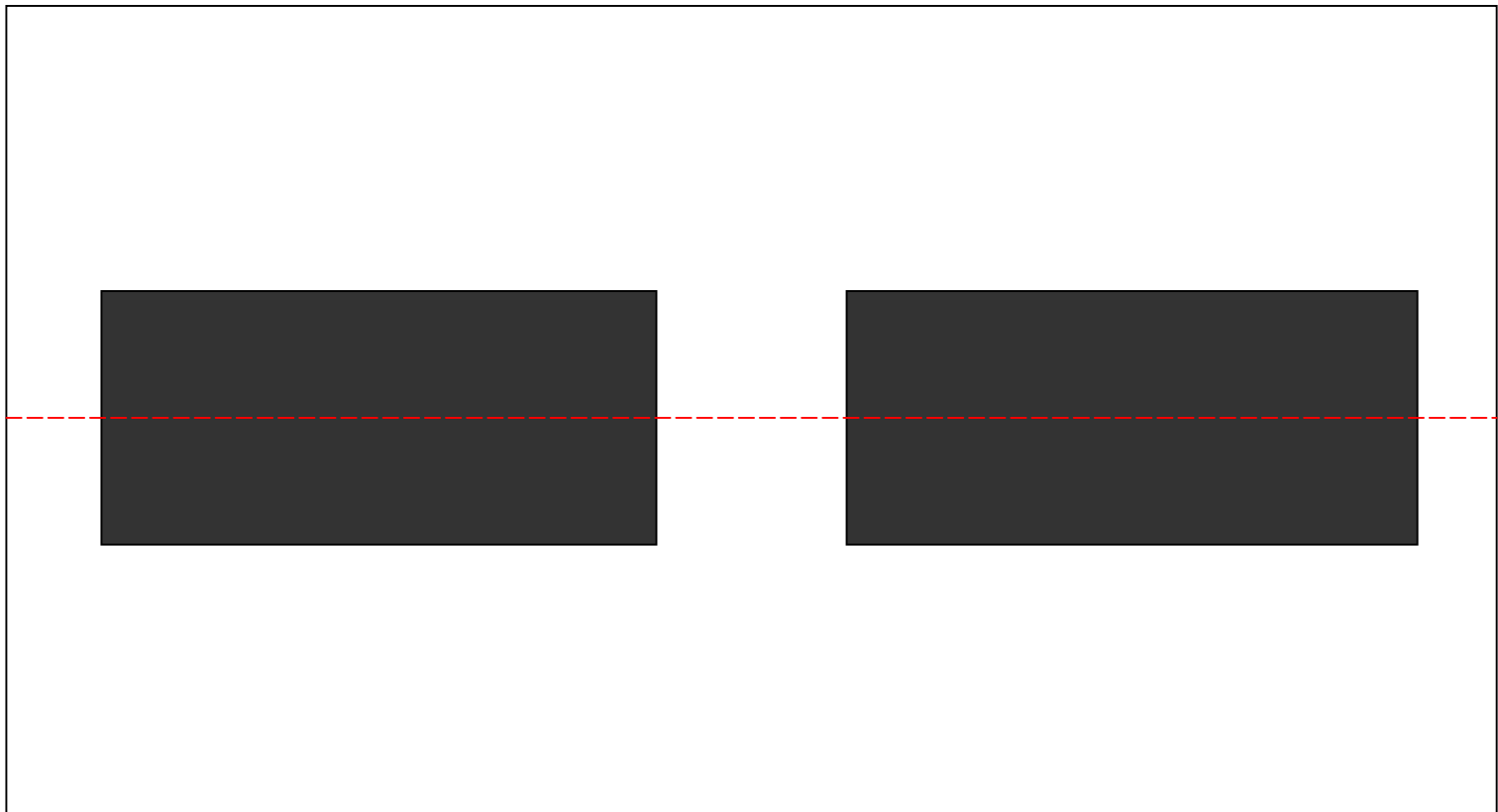
LPCVD Nitride



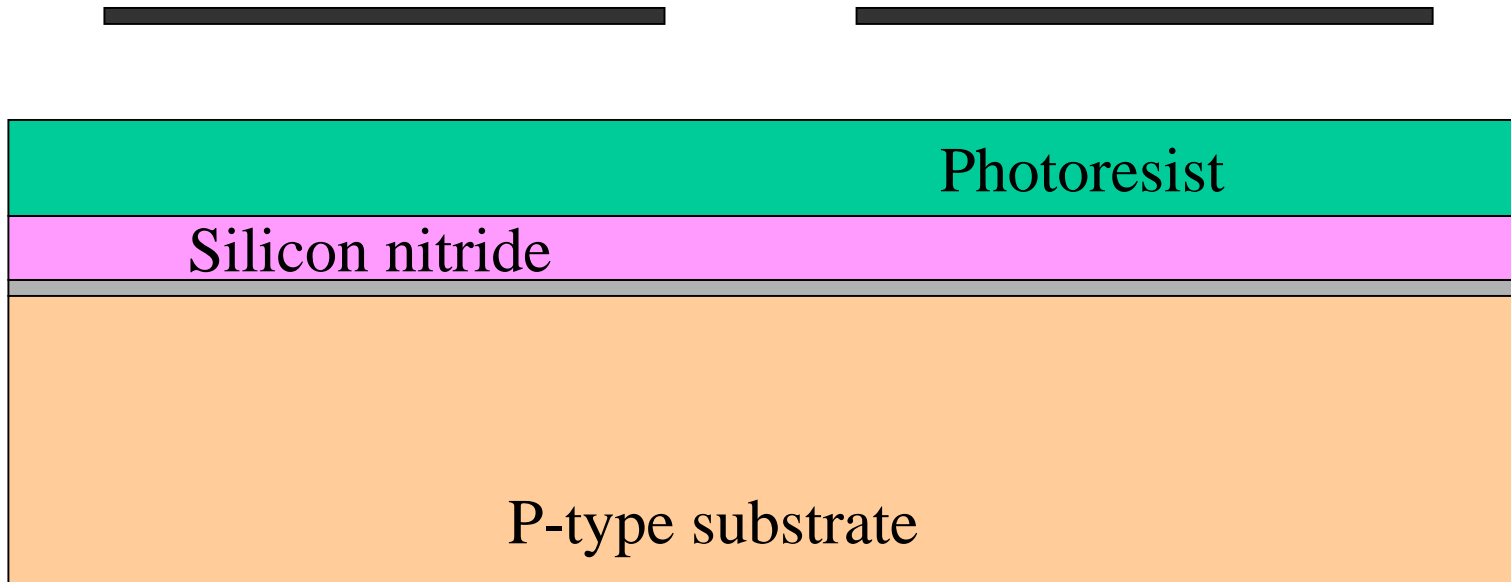
Photoresist Coating



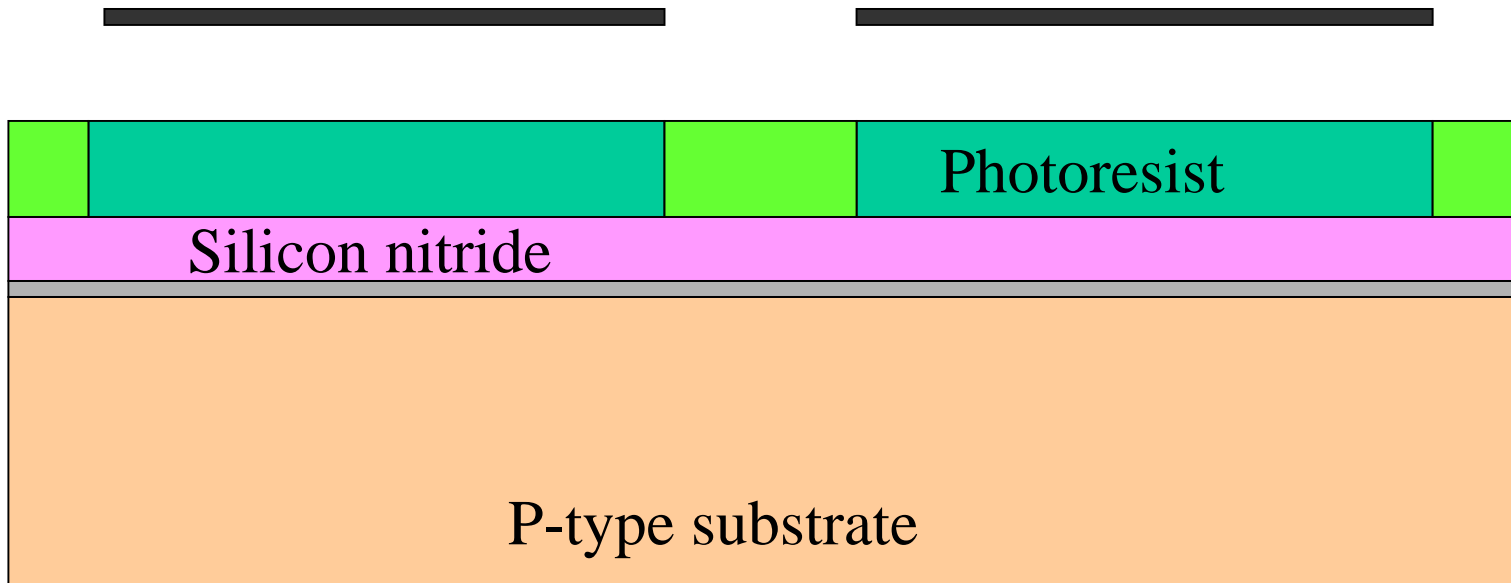
Mask 1 , LOCOS



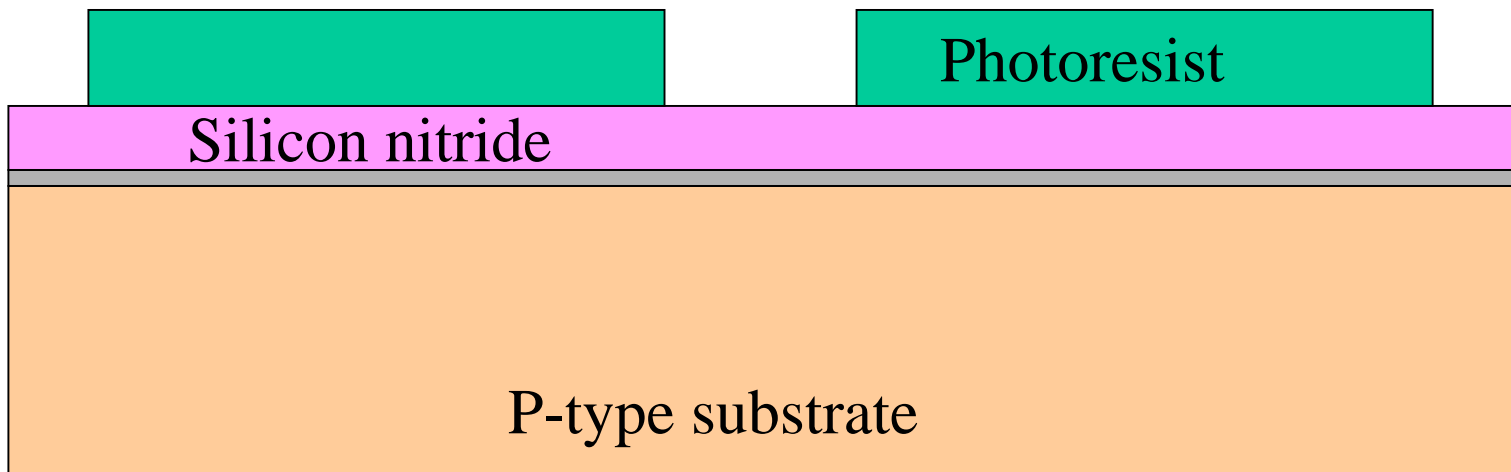
Mask 1 , LOCOS



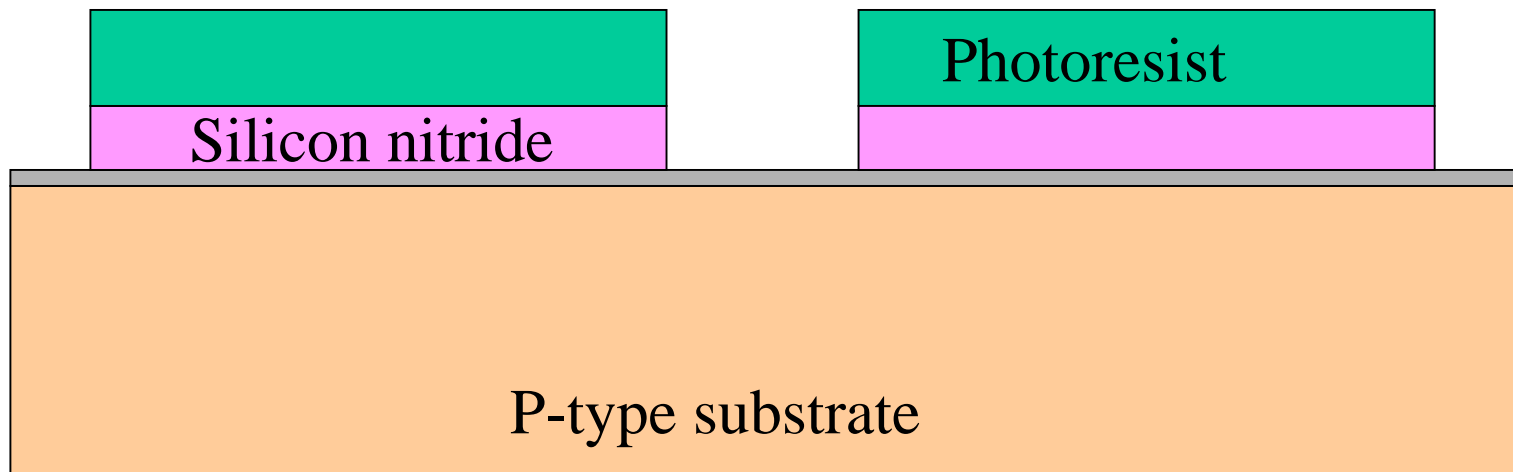
Alignment and Exposure



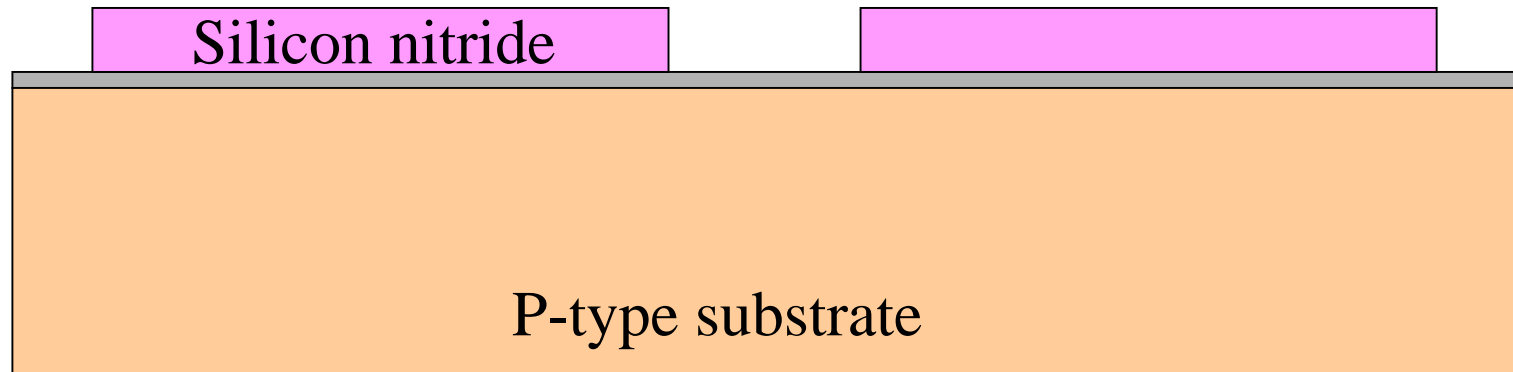
Development



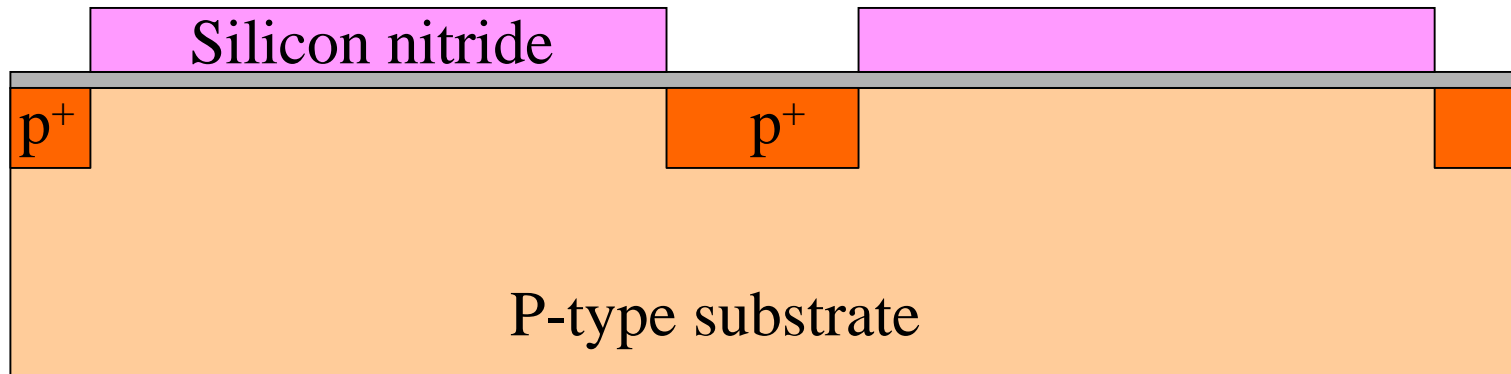
Etch Nitride



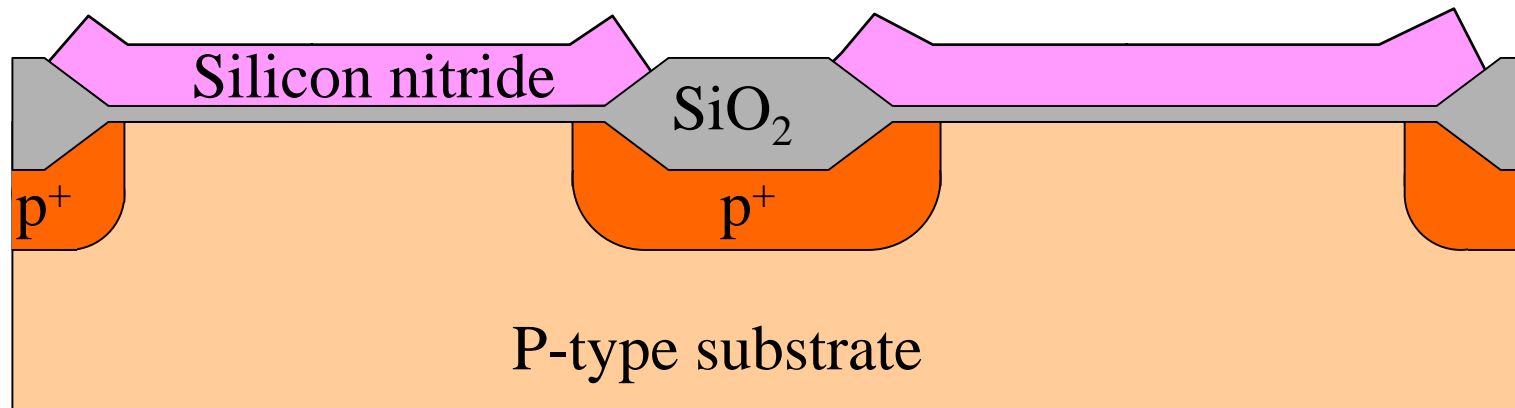
Strip Photoresist



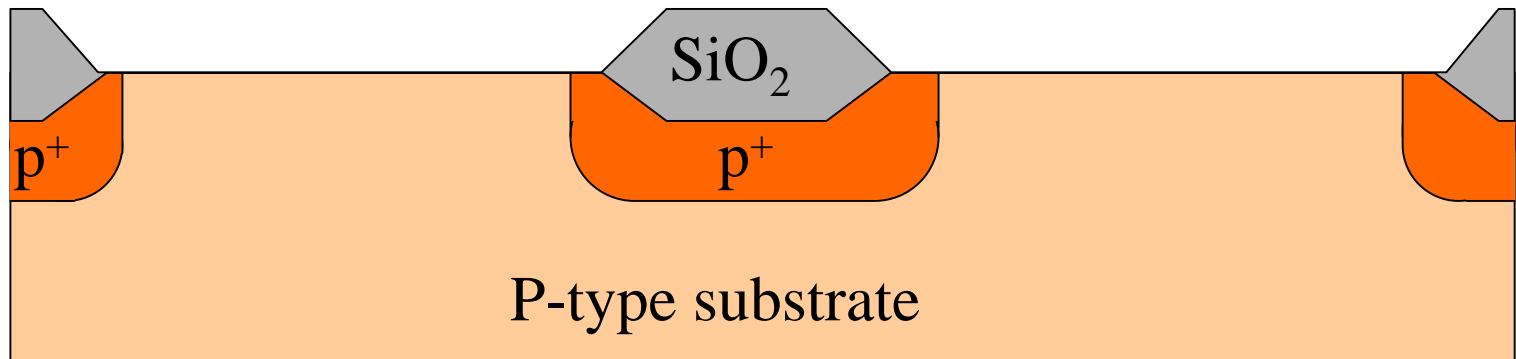
Isolation Implantation



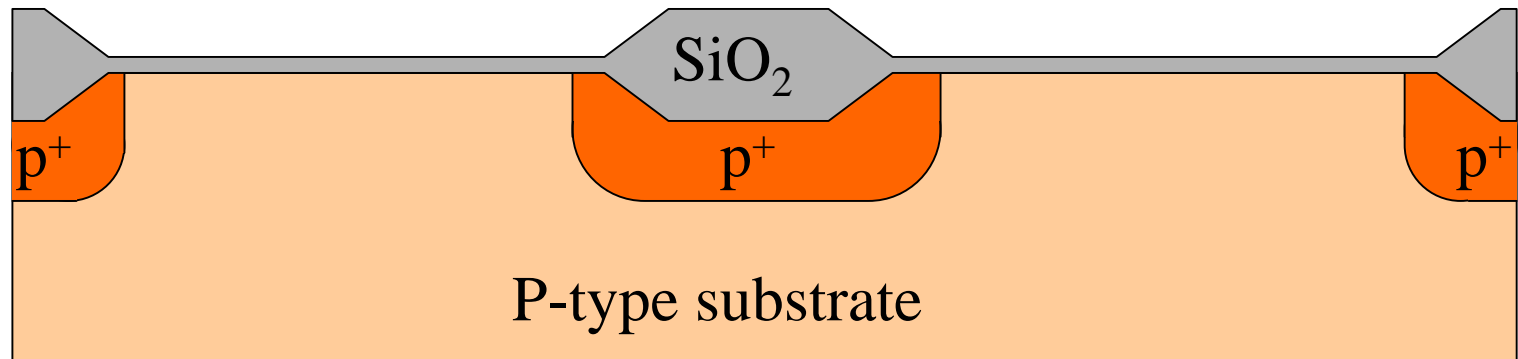
LOCOS Oxidation



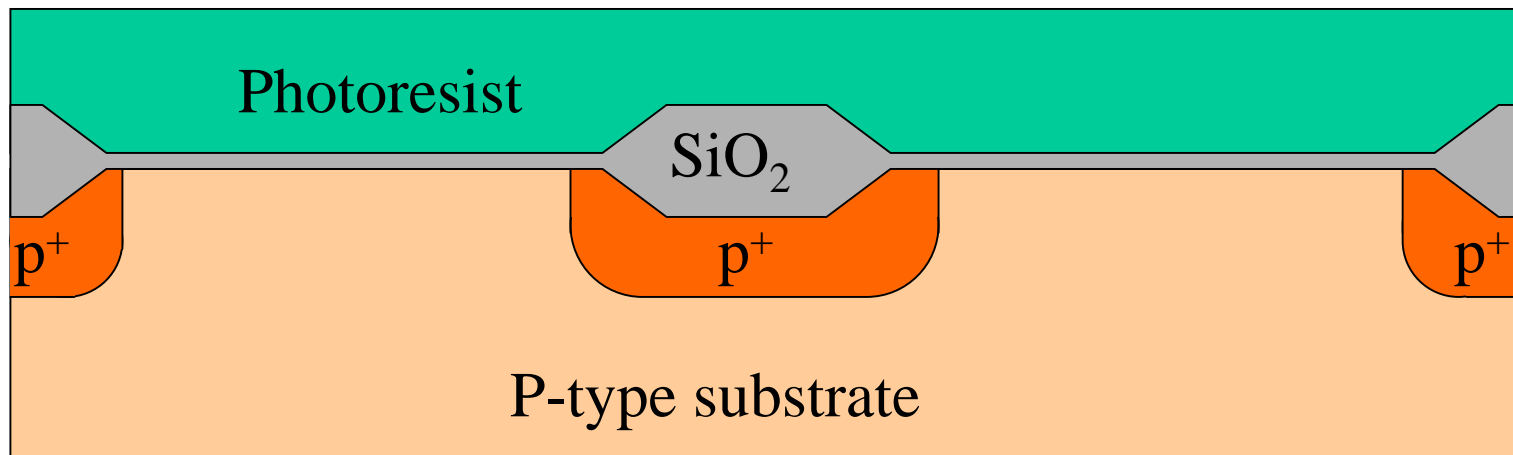
Strip Nitride and Pad Oxide , Clean



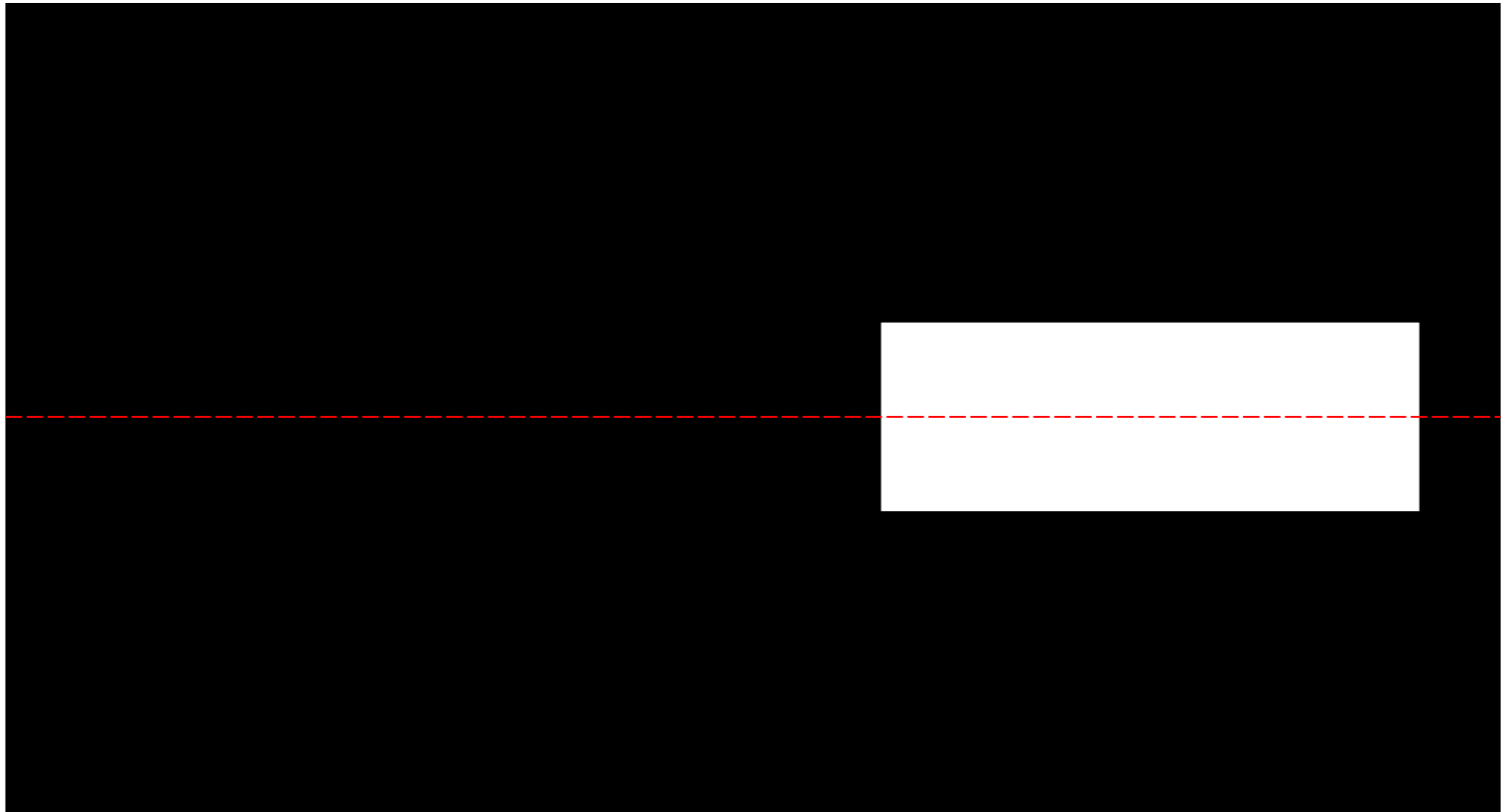
Screen Oxidation



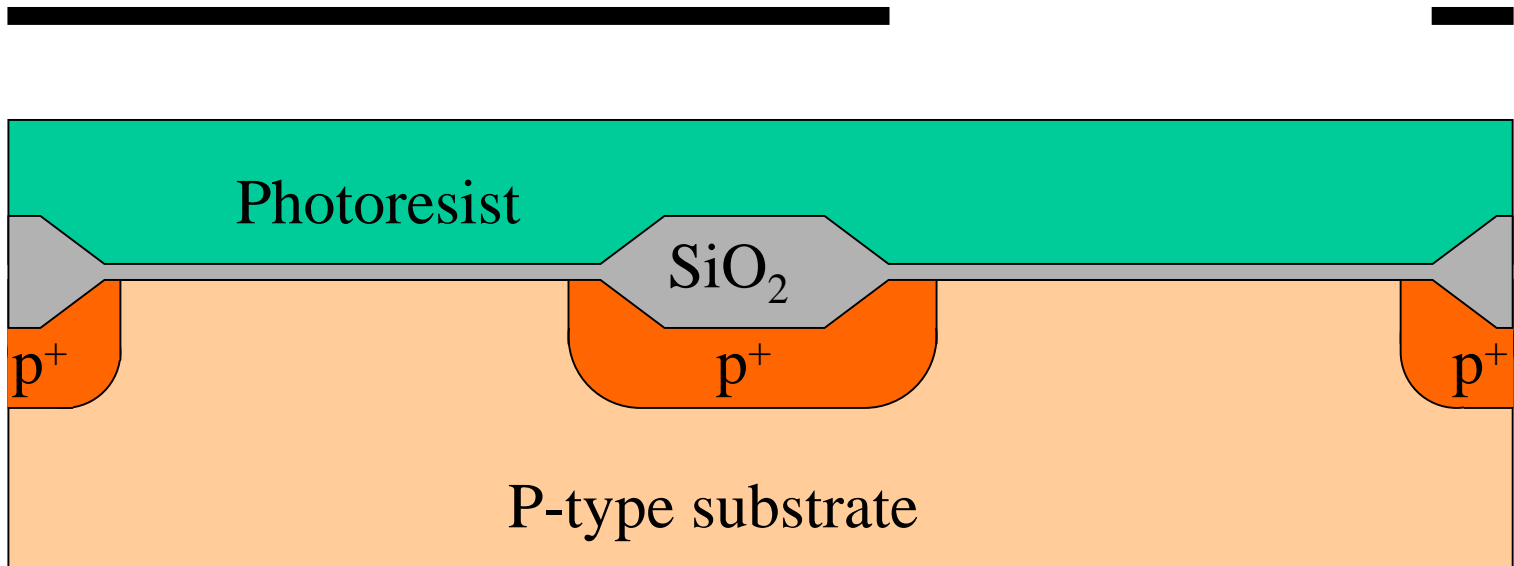
Photoresist Coating



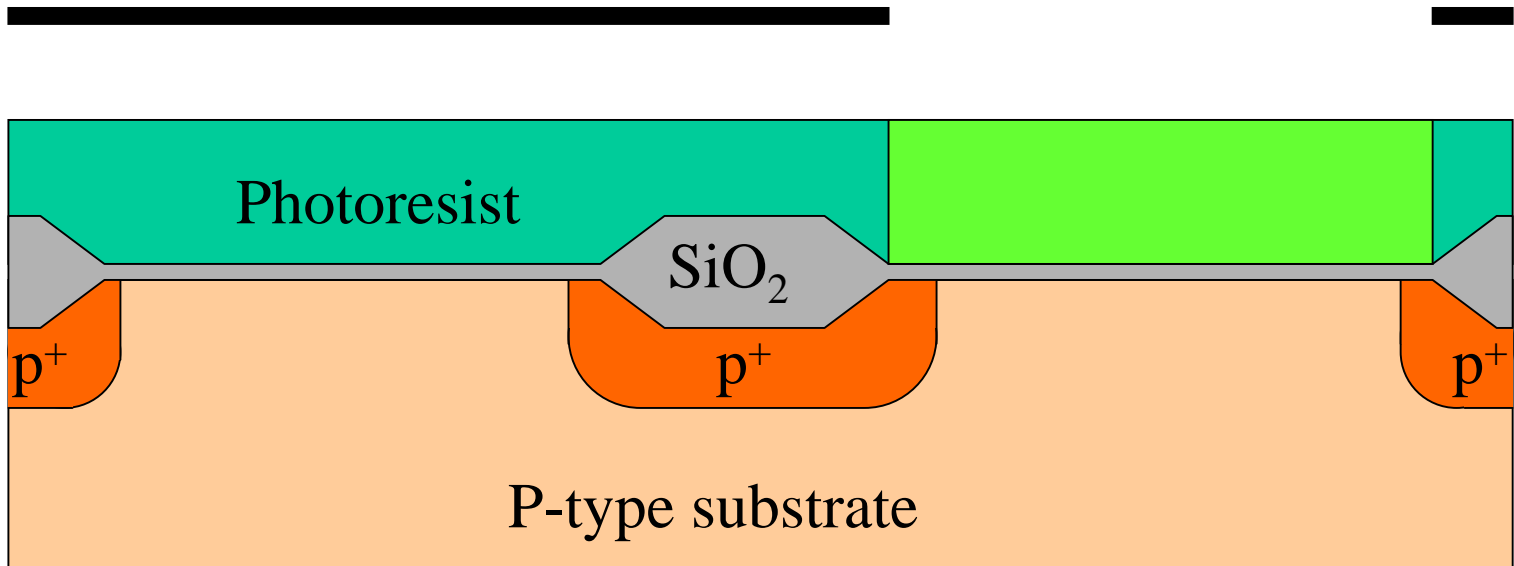
Mask 2 , N-well



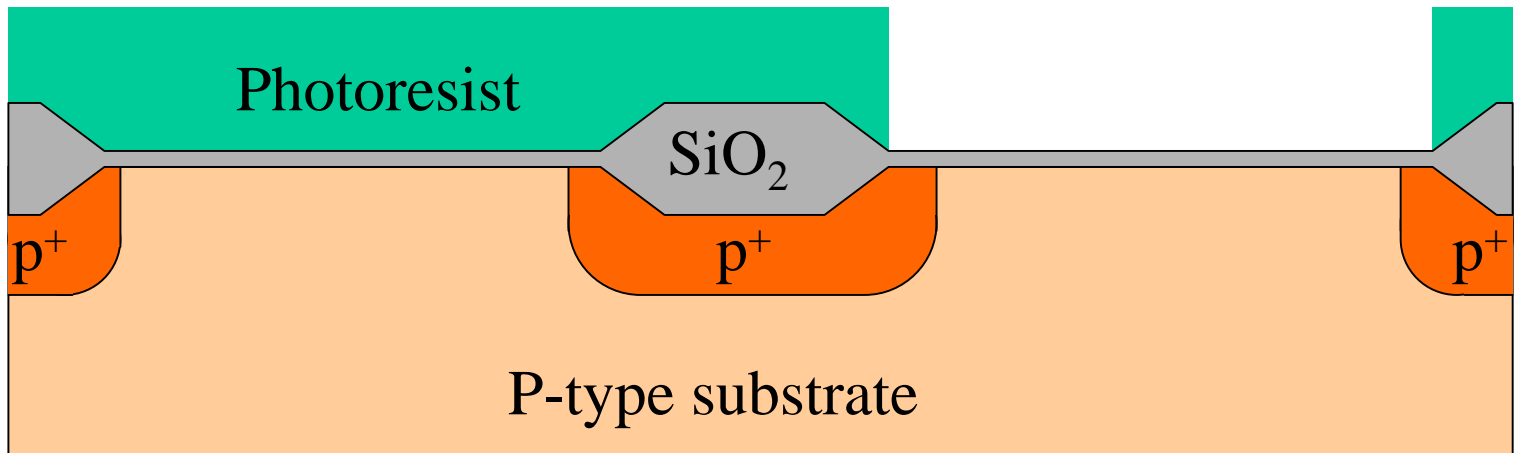
Mask 2 , N-well



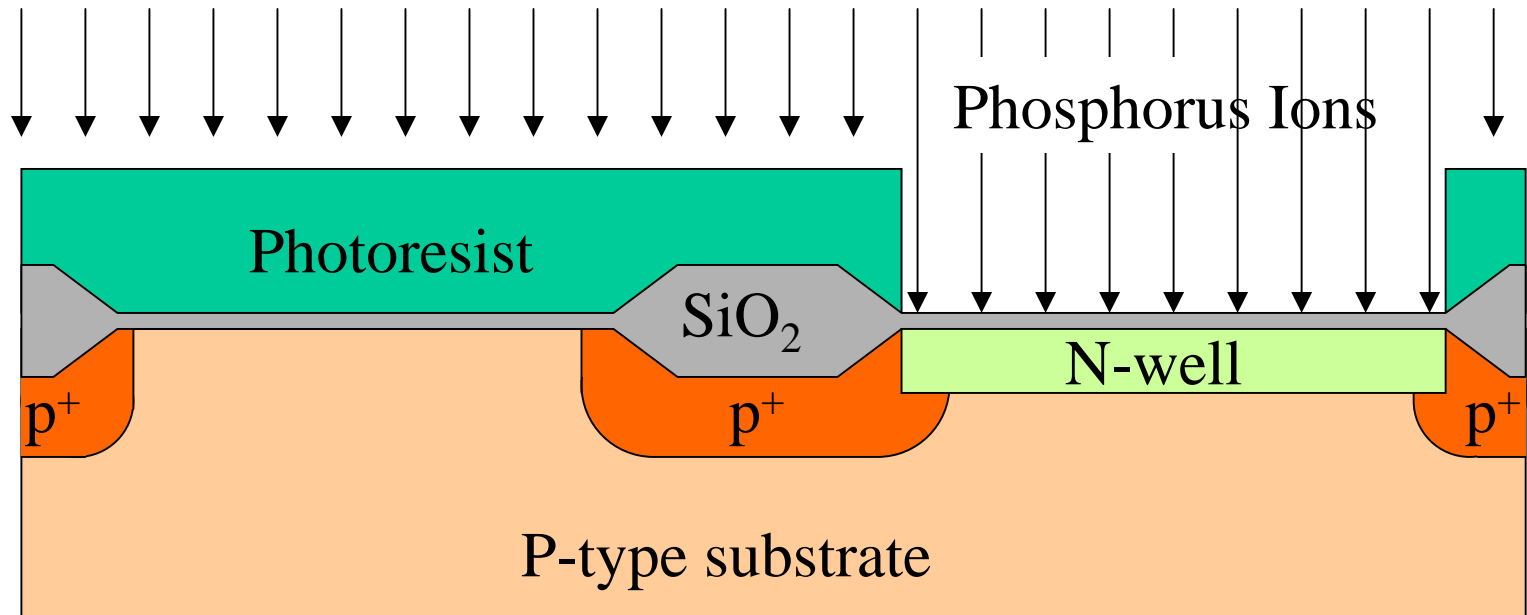
Exposure



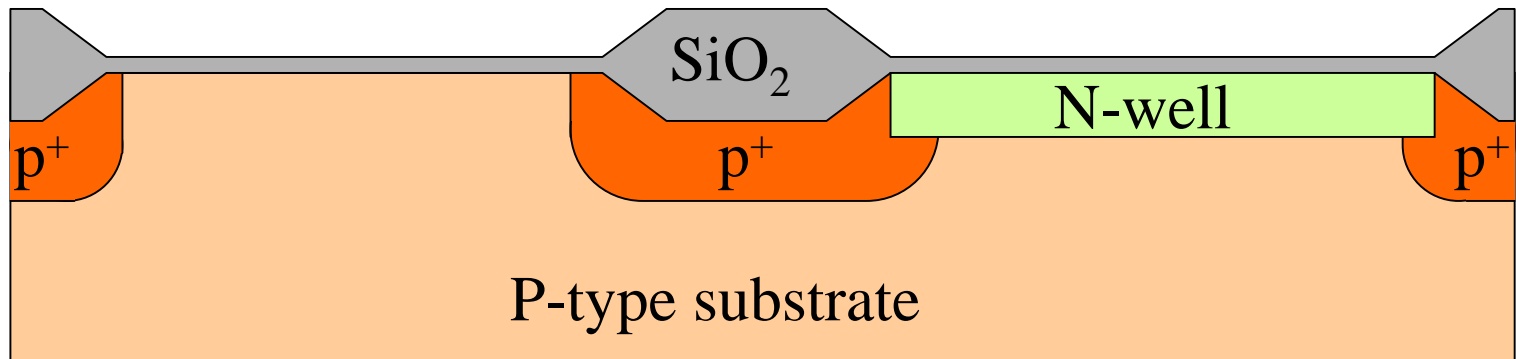
Development



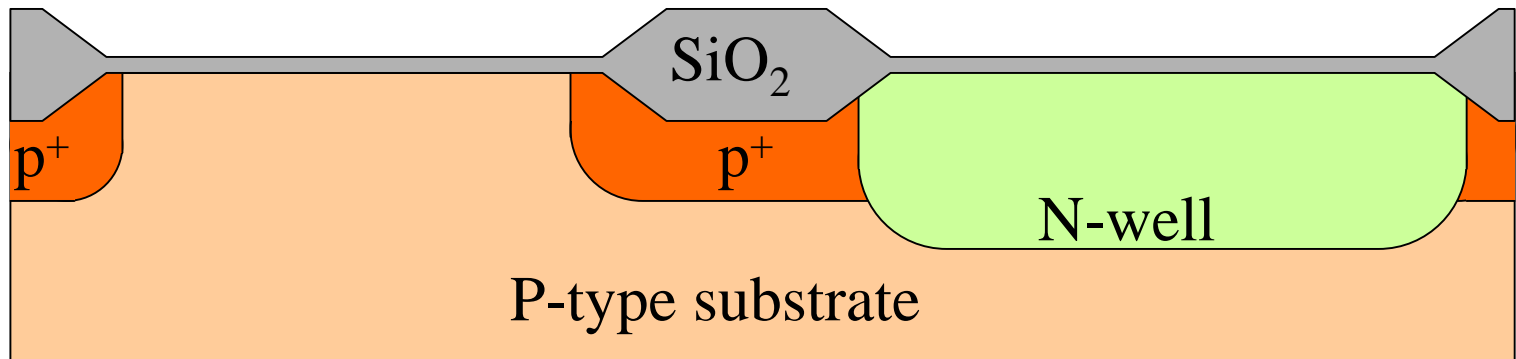
N-well Implantation



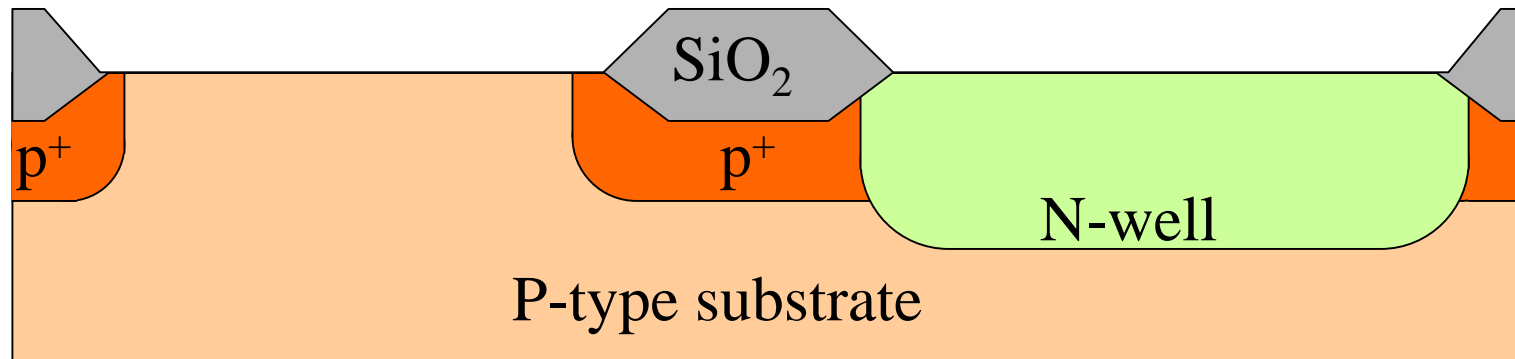
Strip Photoresist



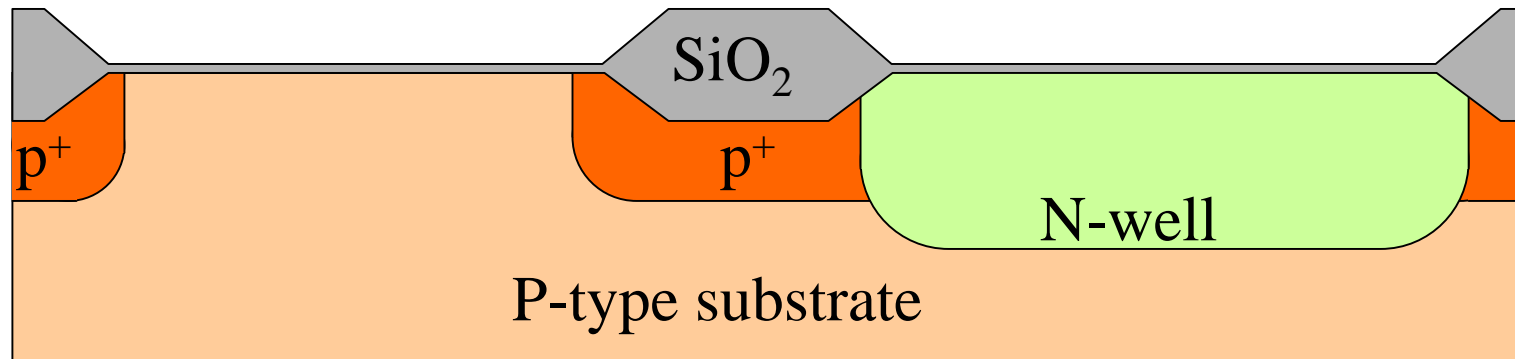
N-well Drive-in



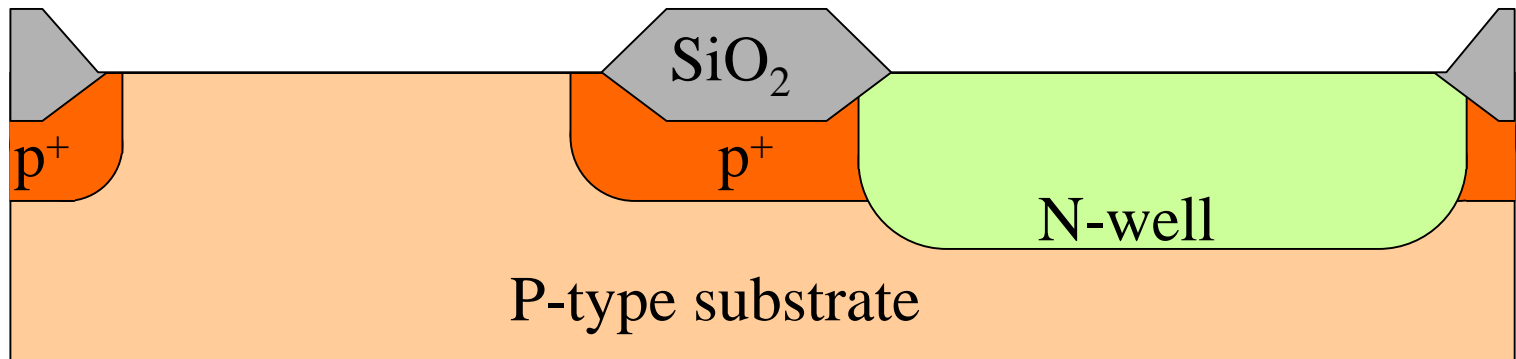
Strip Screen Oxide



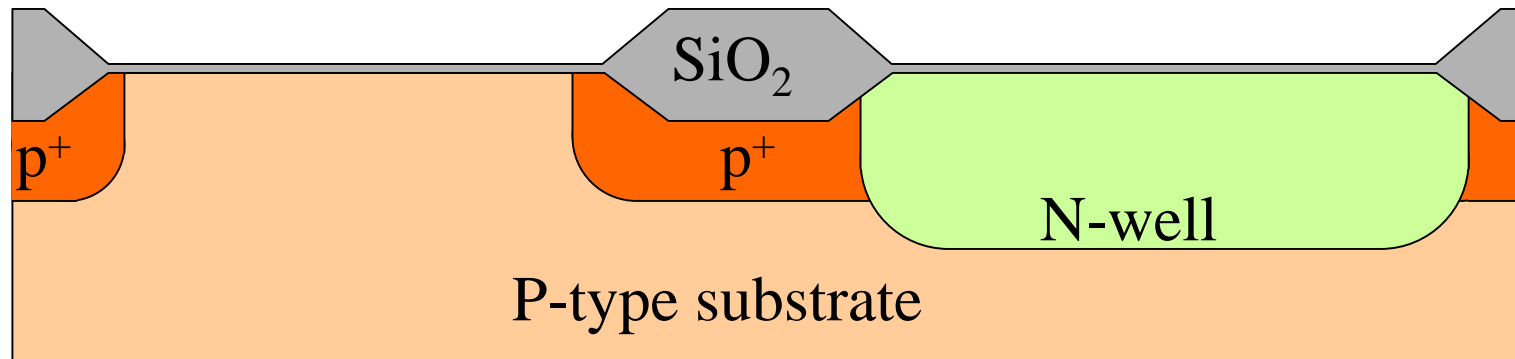
Grow Sacrificial Oxide



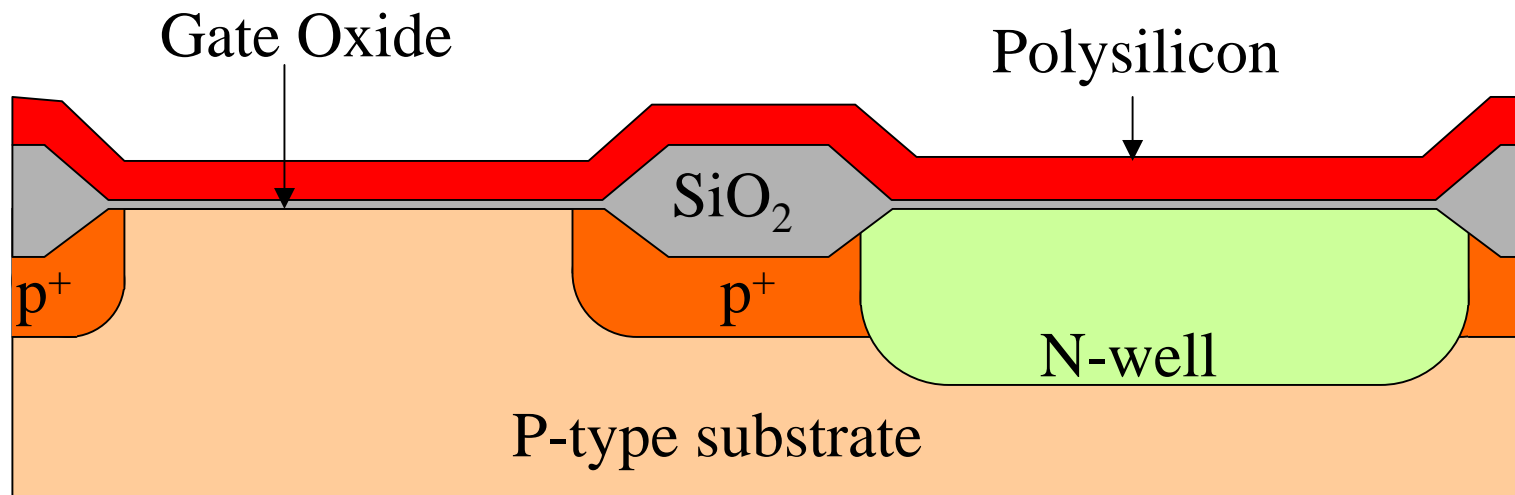
Strip Sacrificial Oxide



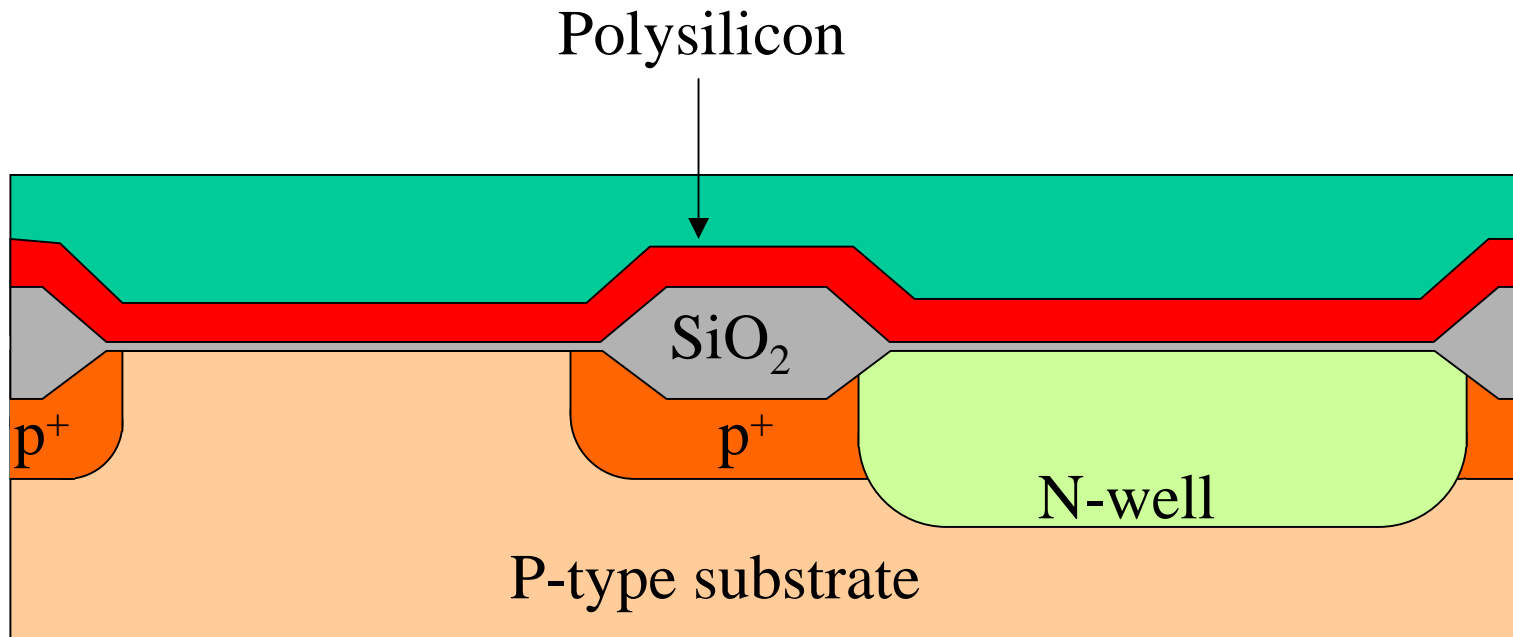
Grow Gate Oxide



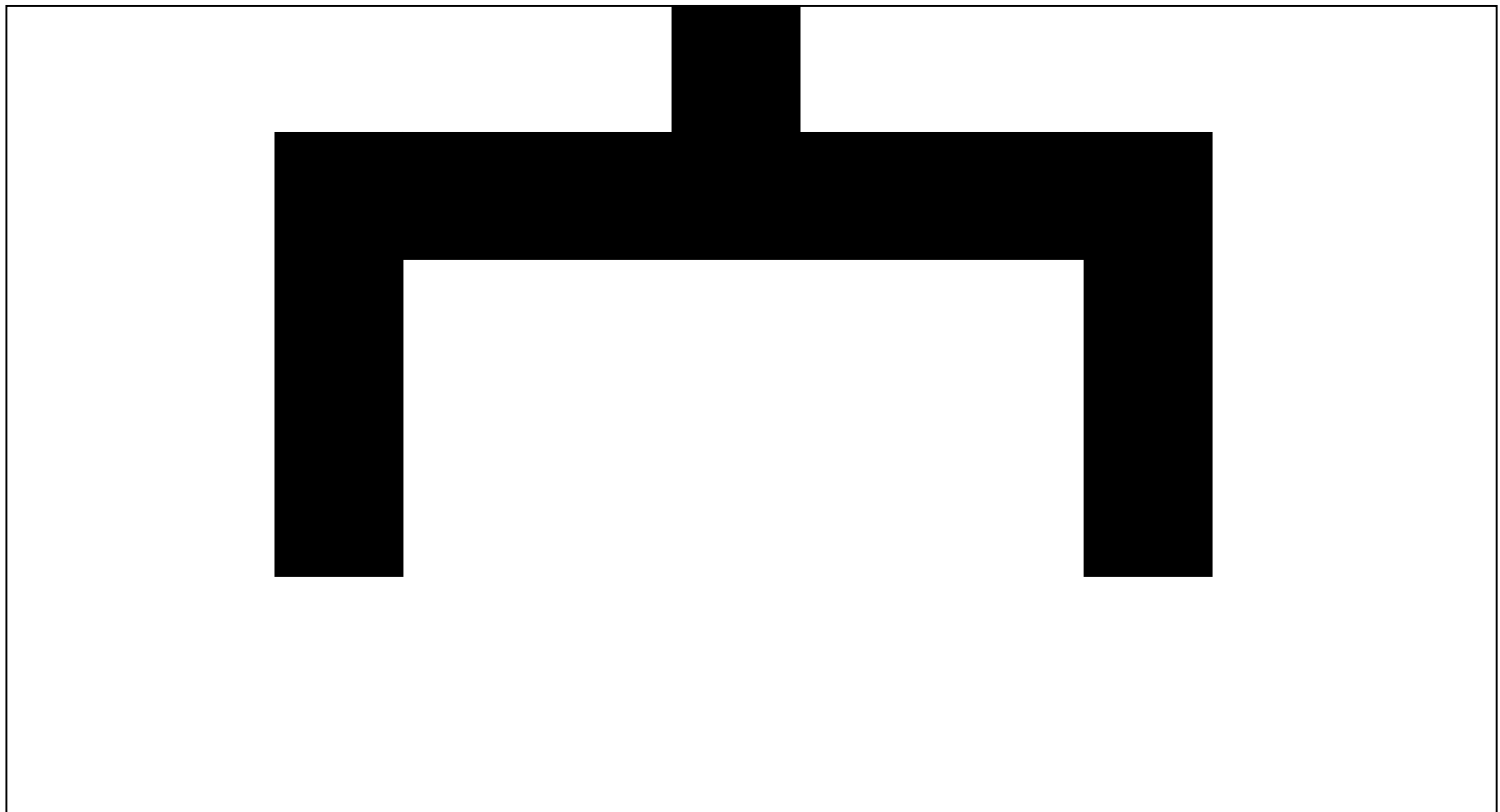
Deposit Polysilicon



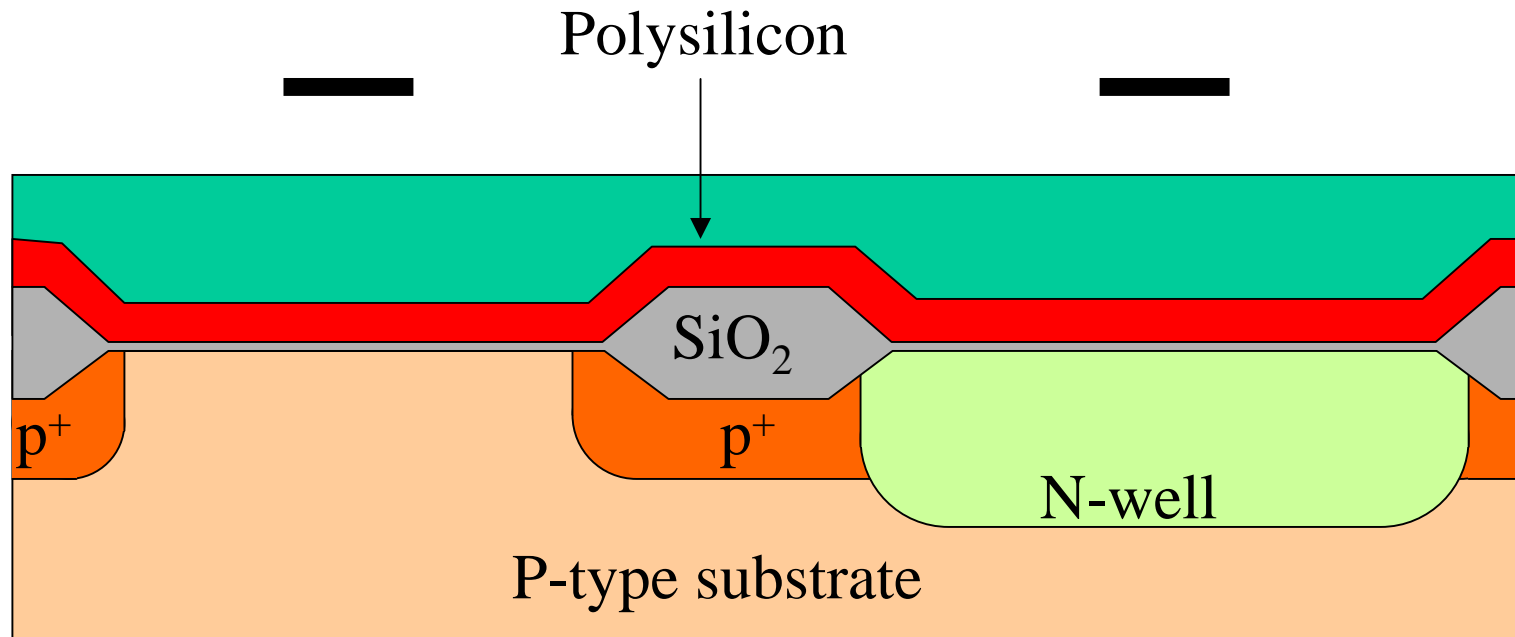
Photoresist Coating



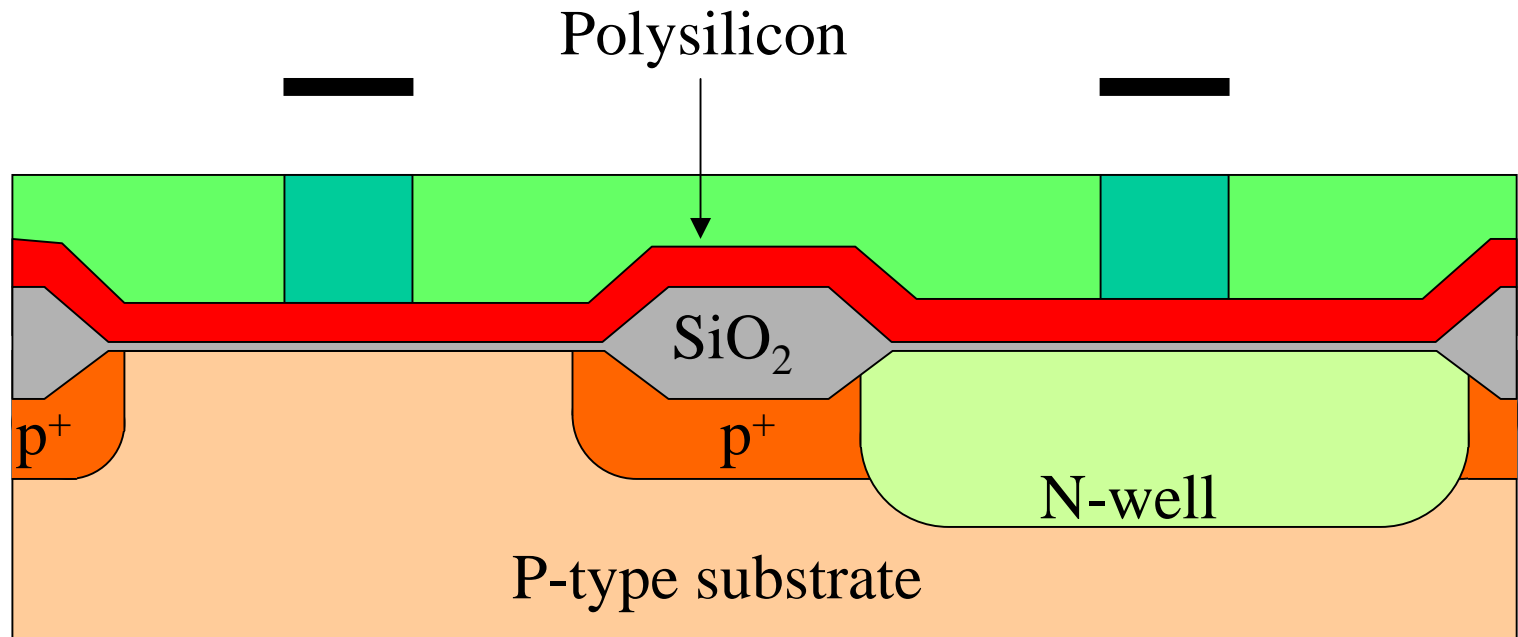
Mask 3 , Gate and Local Interconnection



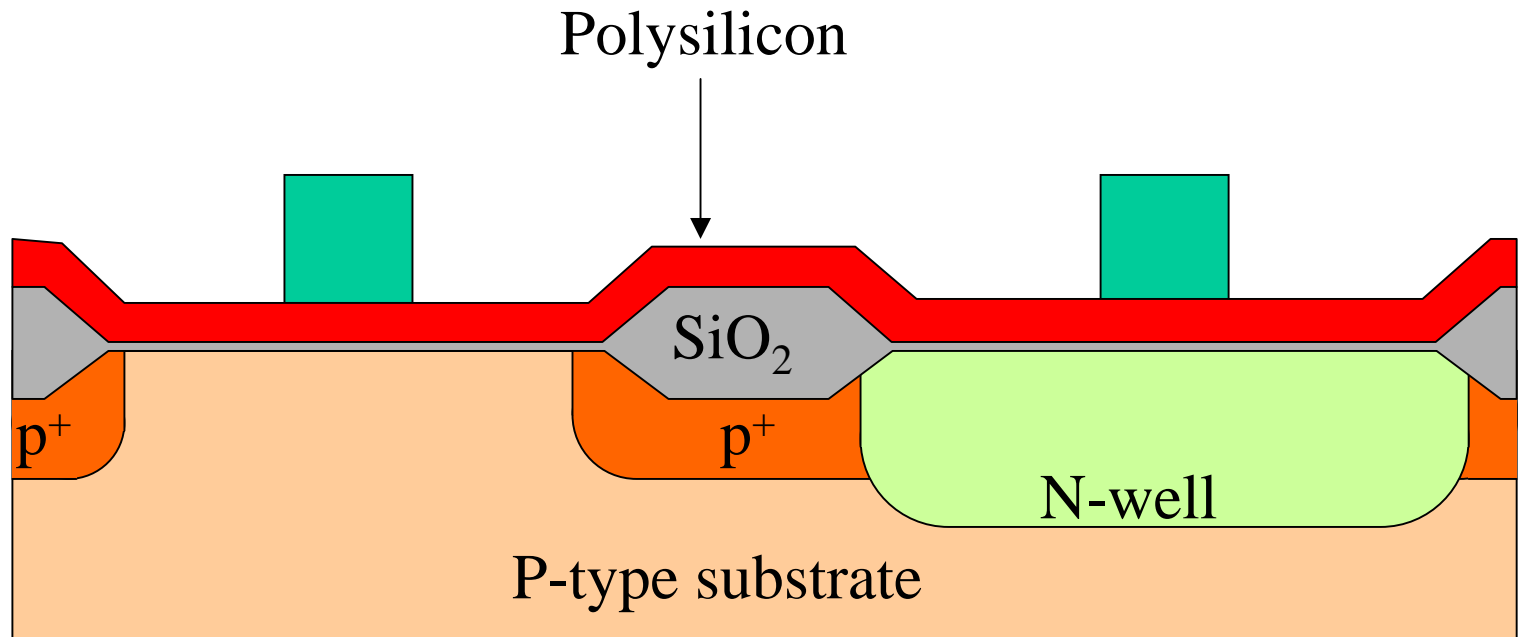
Mask 3 , Gate and Local Interconnection



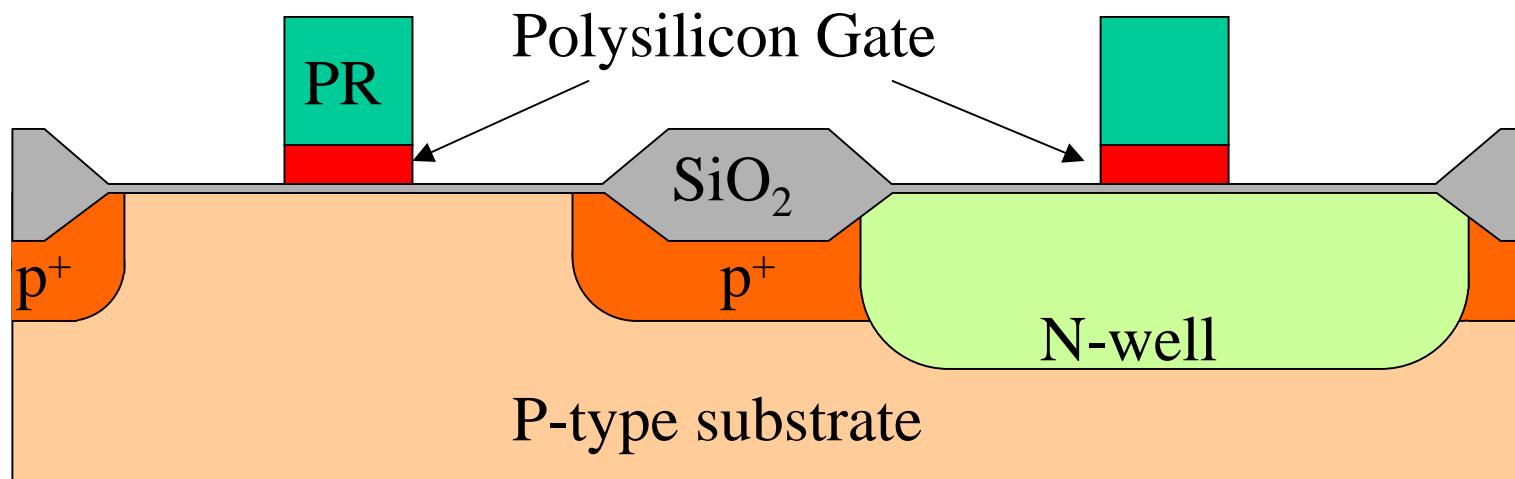
Exposure



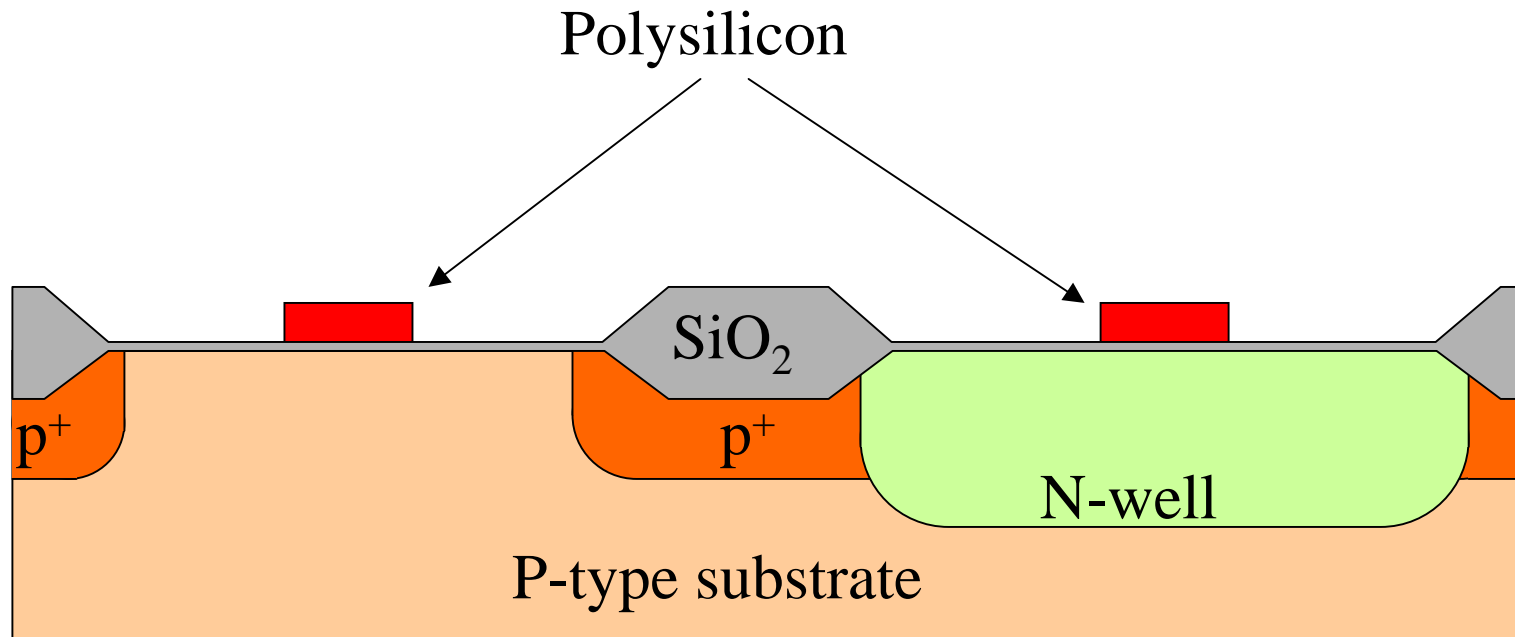
Development



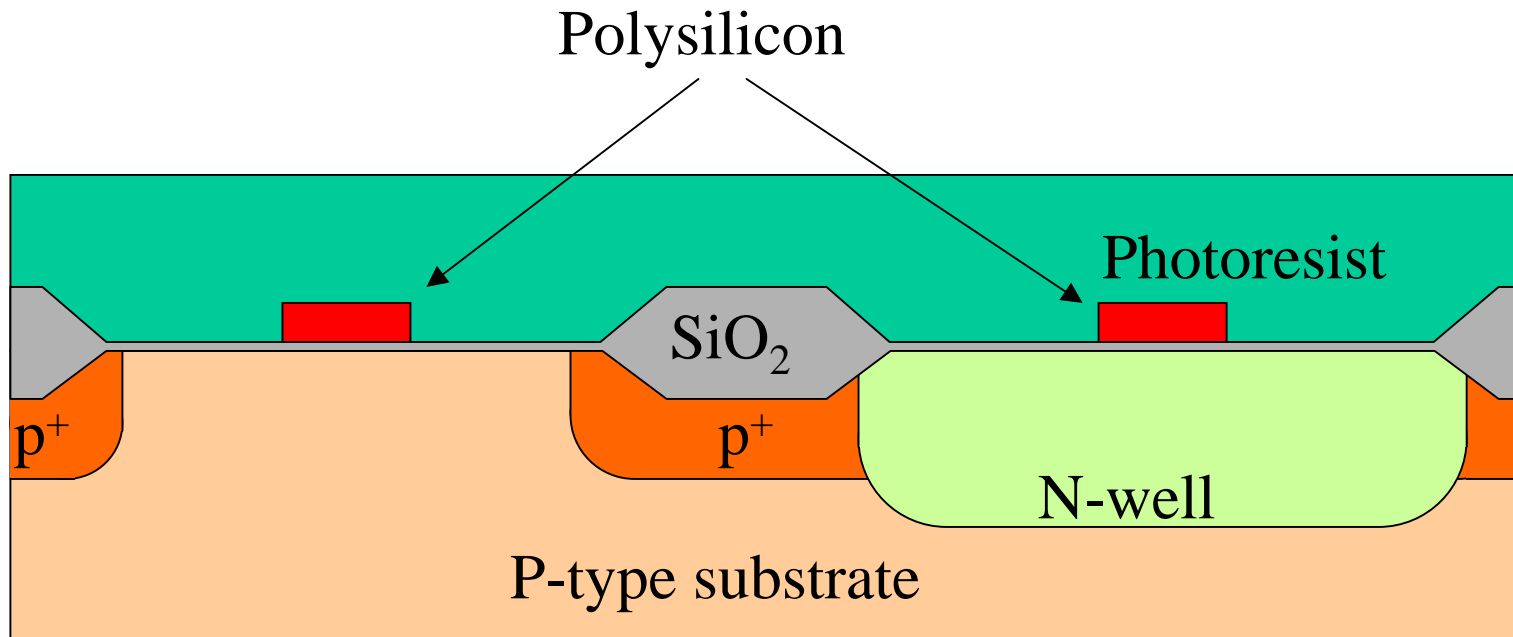
Etch Polysilicon



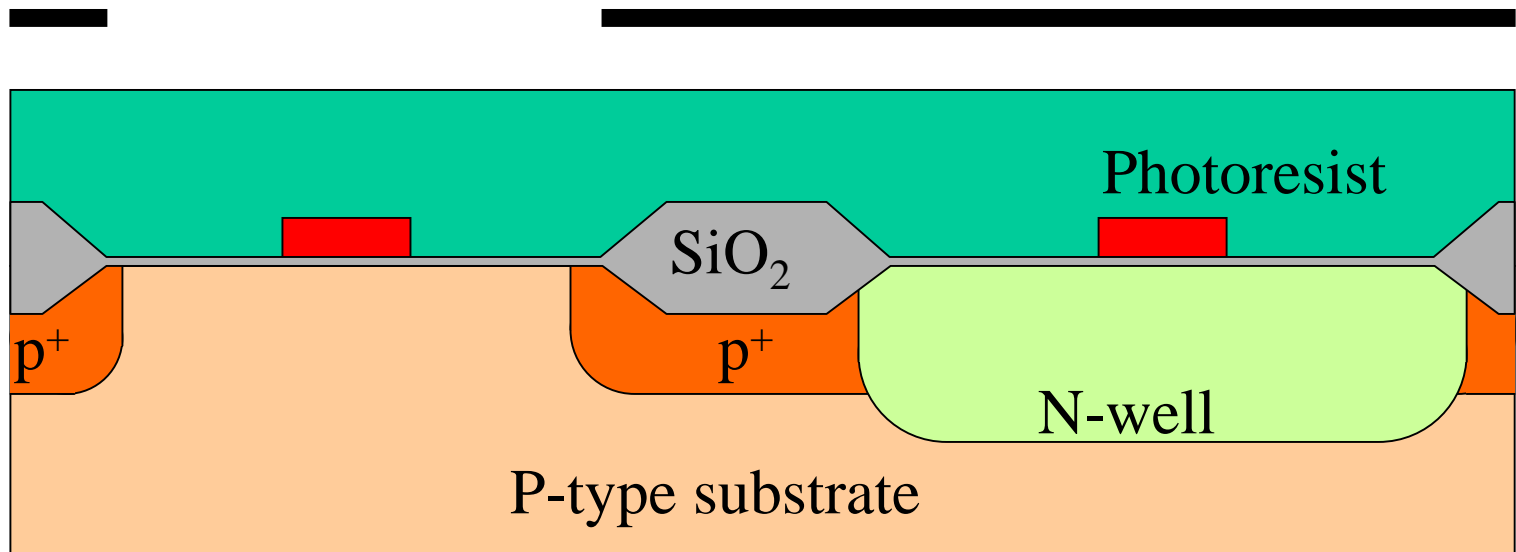
Strip Photoresist



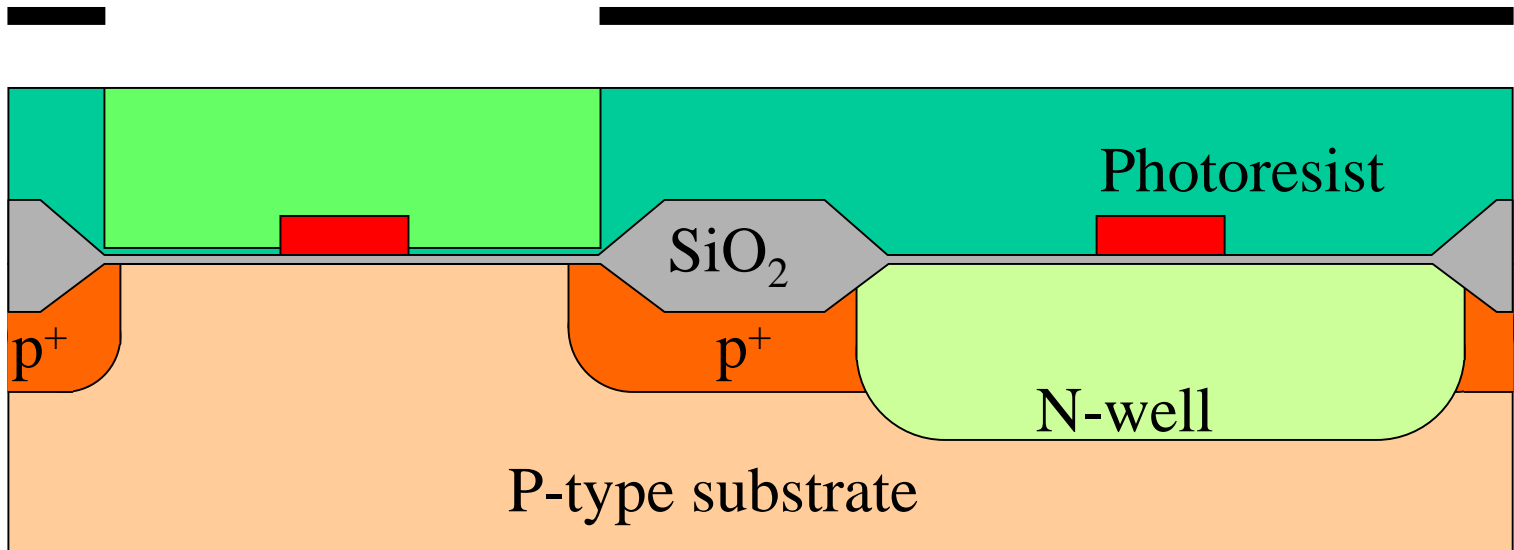
Photoresist Coating



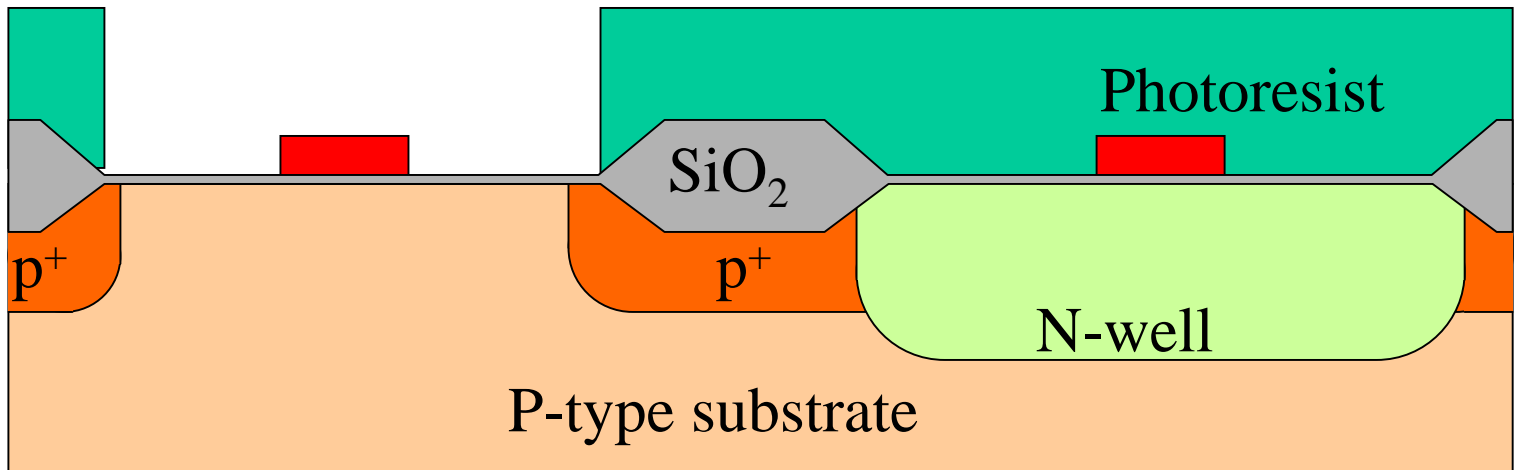
Mask 4 , n-Source/Drain



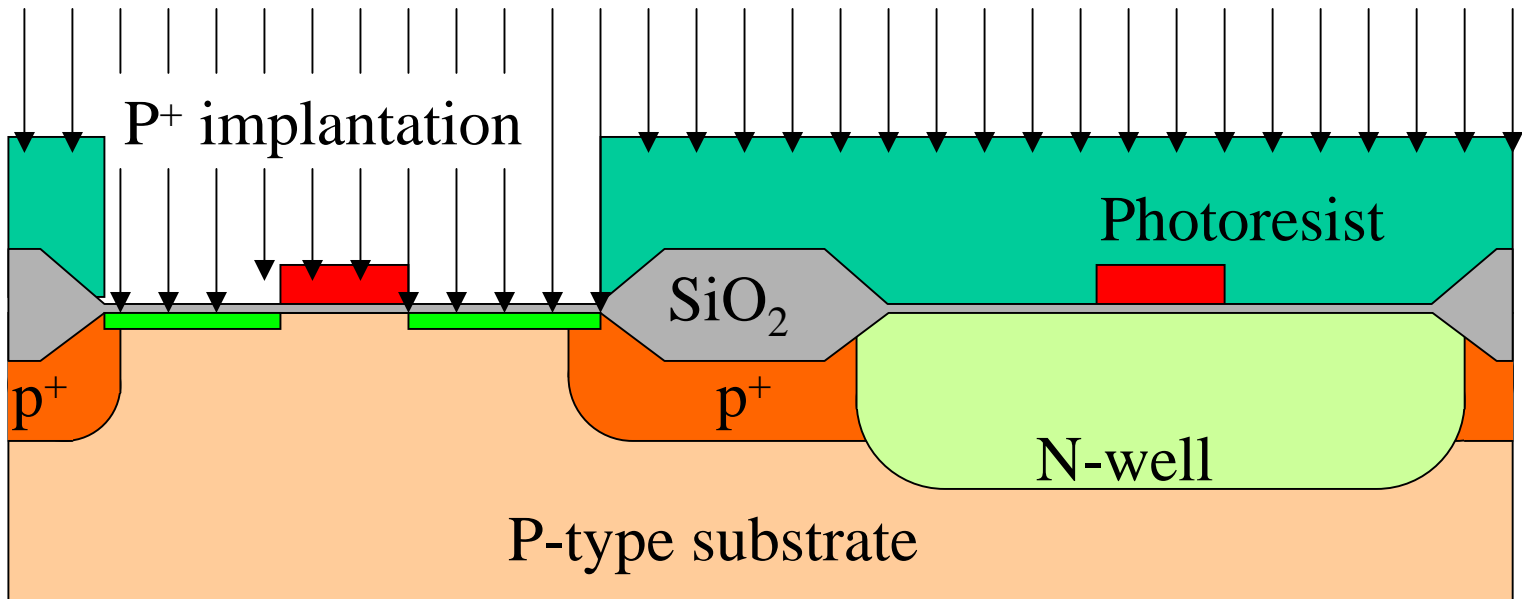
Exposure



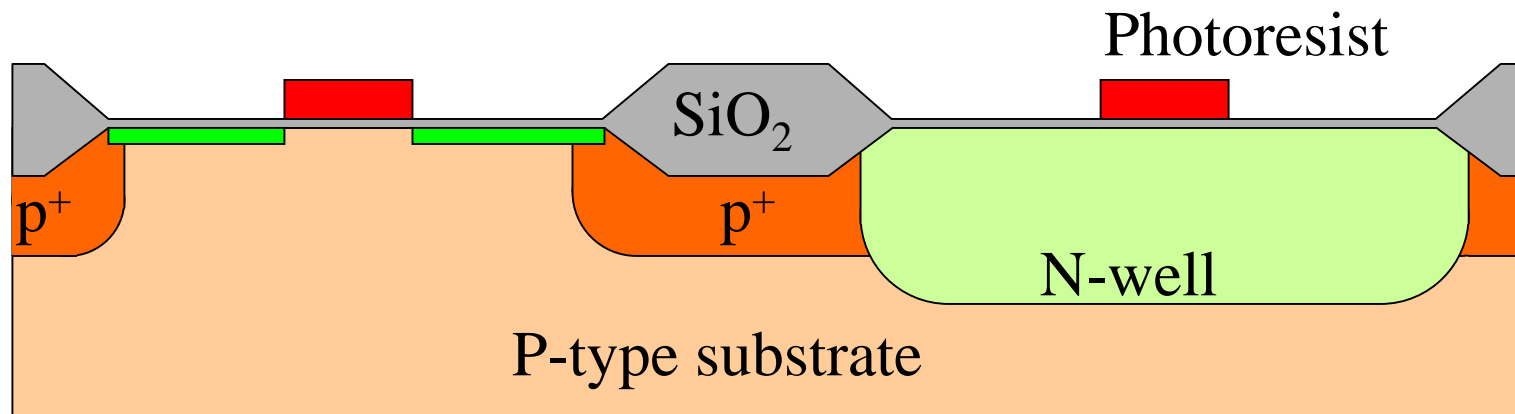
Development



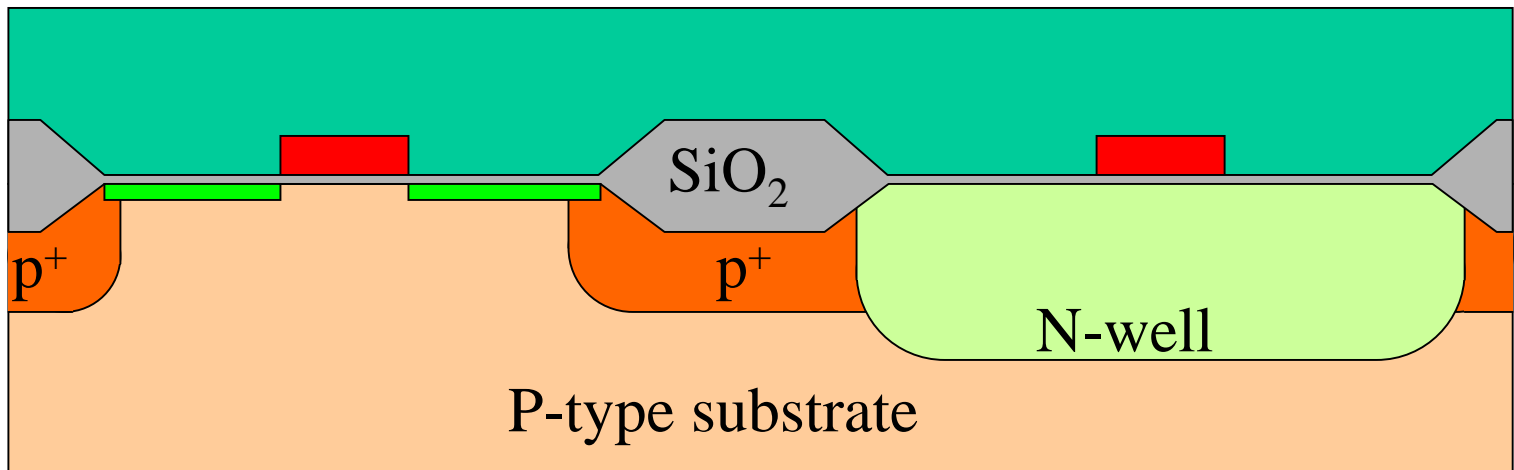
N-Source/Drain Ion Implantation



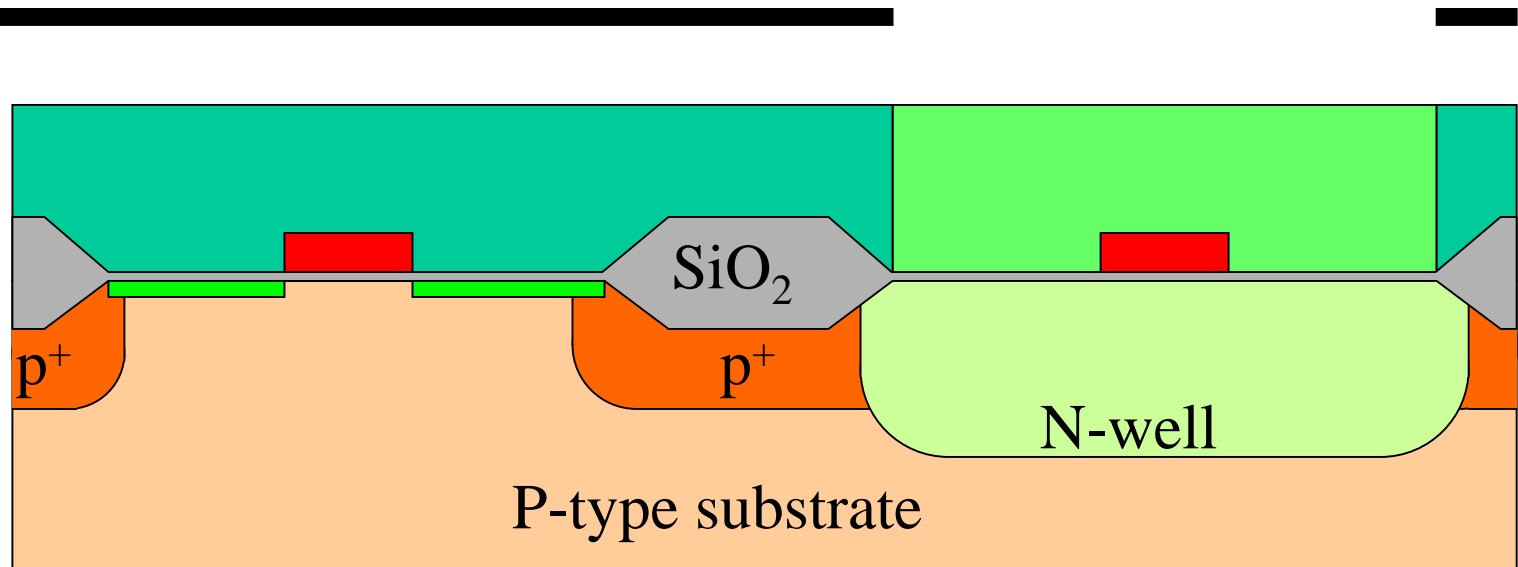
Strip Photoresist



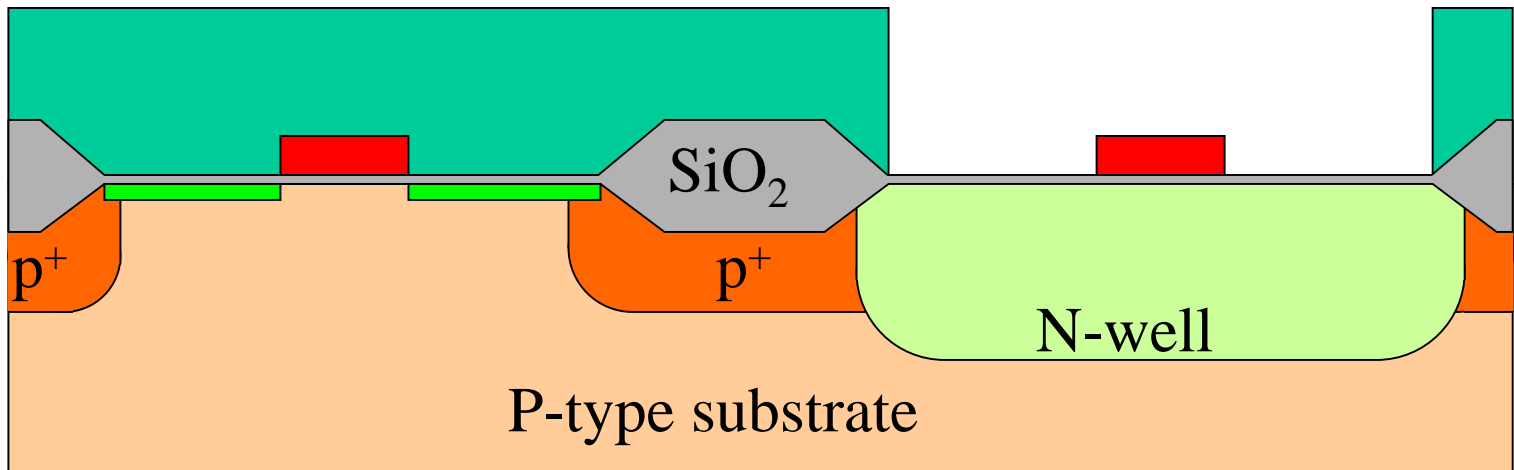
Photoresist Coating



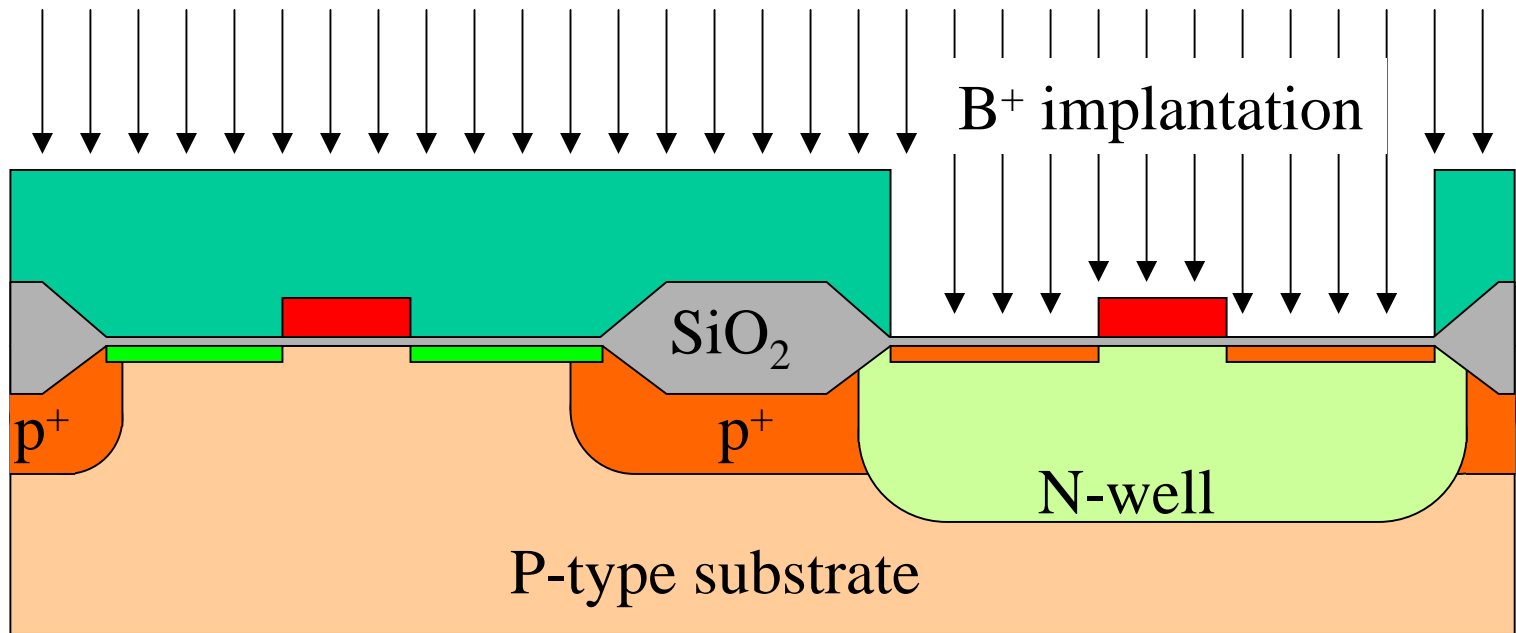
Mask 5 , P-Source/Drain Exposure



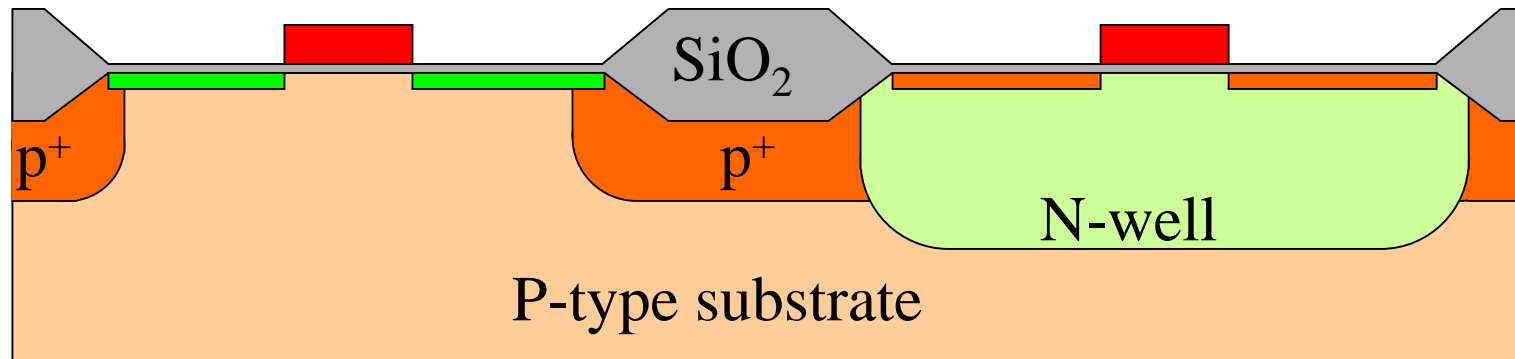
Development



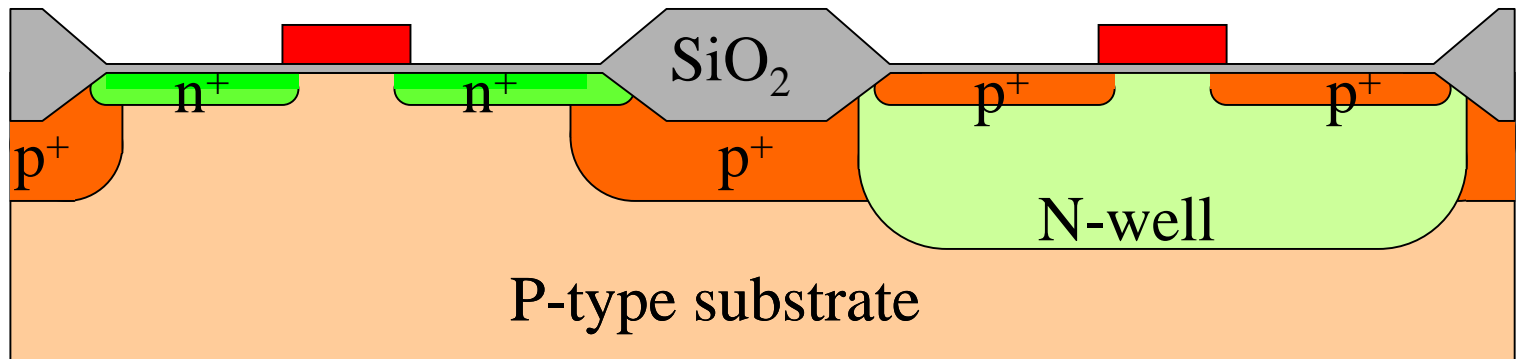
P-Source/Drain Implantation



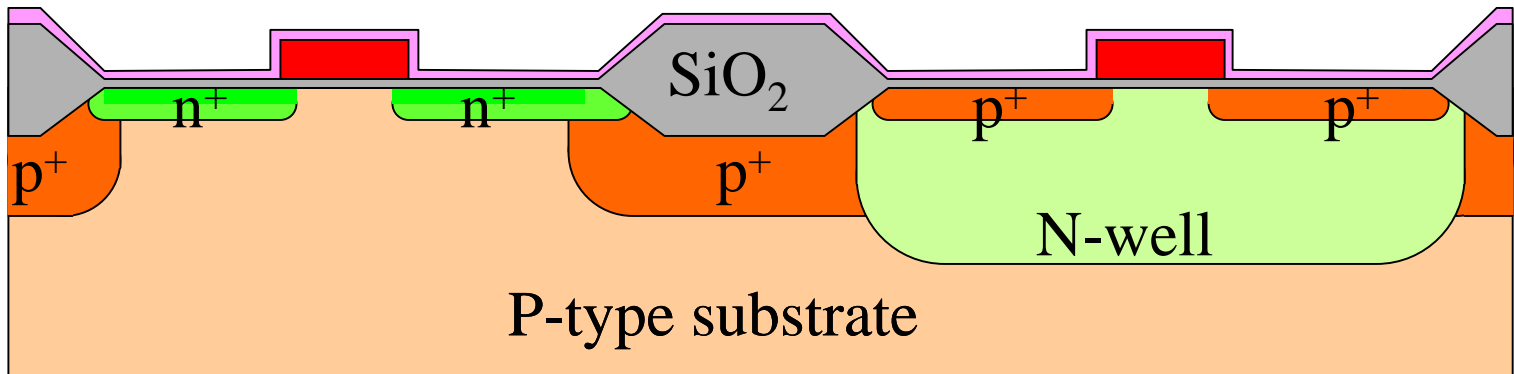
Strip Photoresist



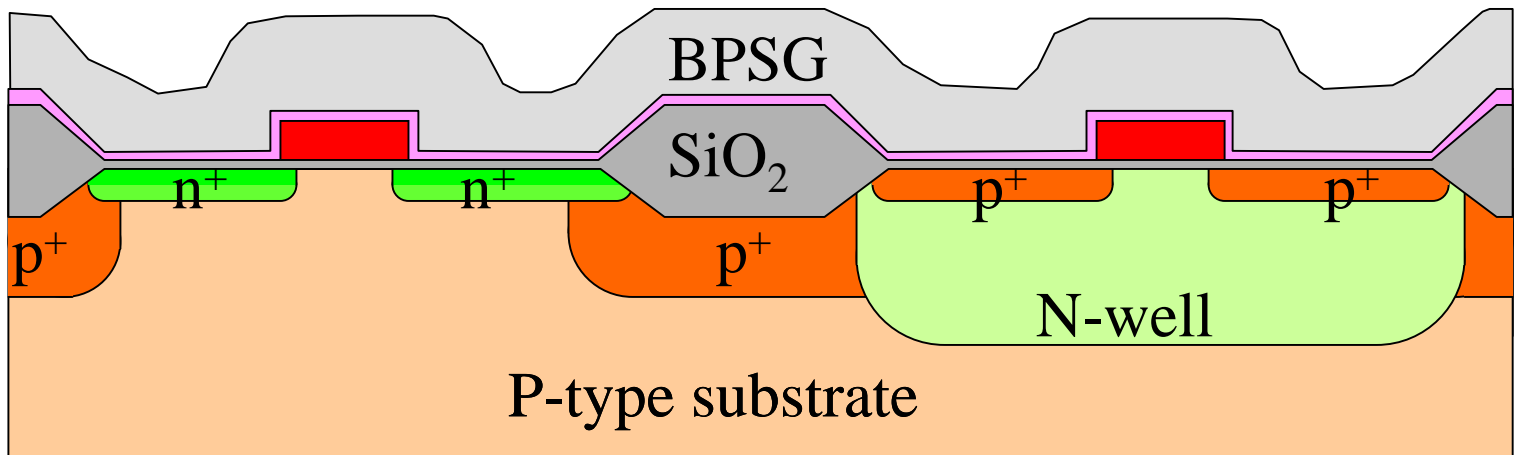
Anneal



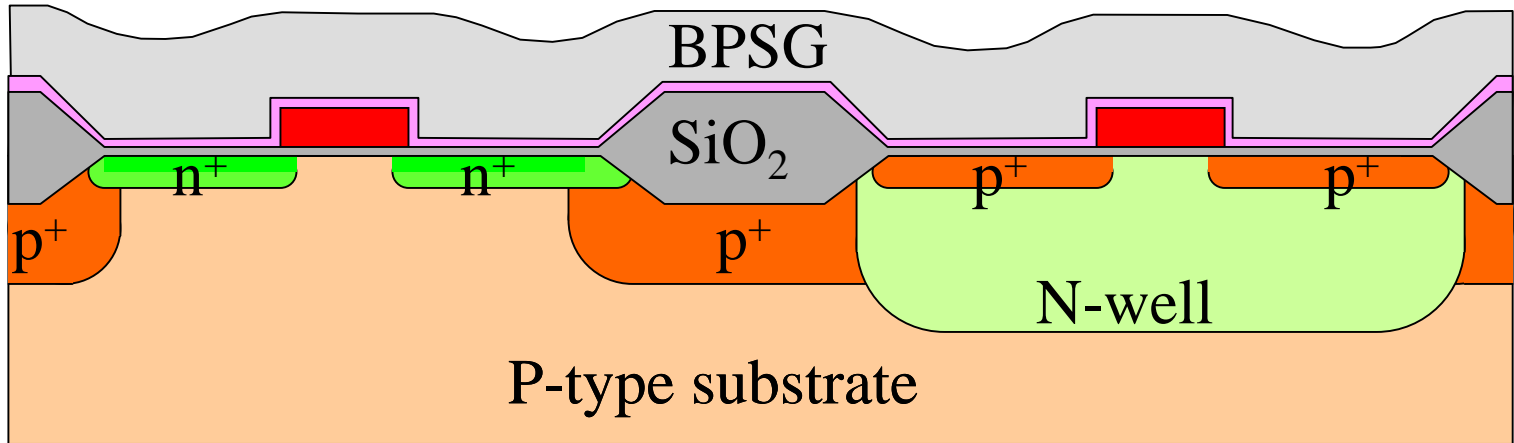
LPCVD Barrier Nitride



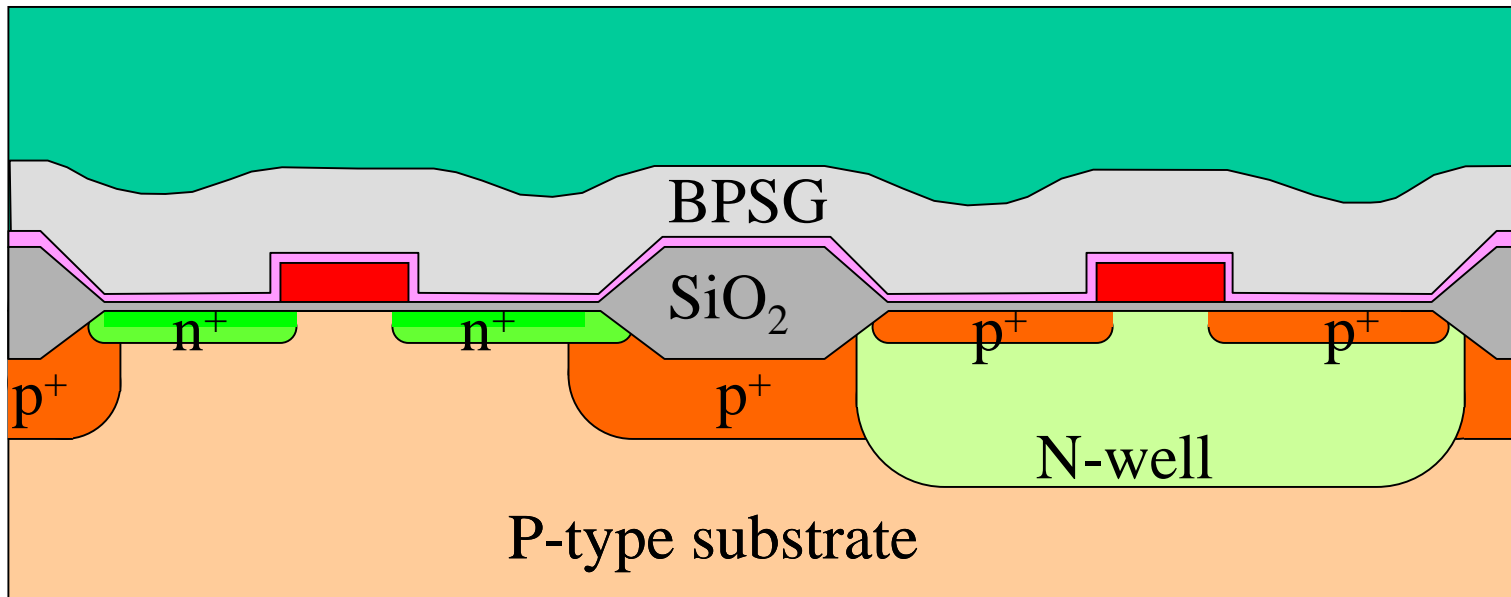
CVD BPSG



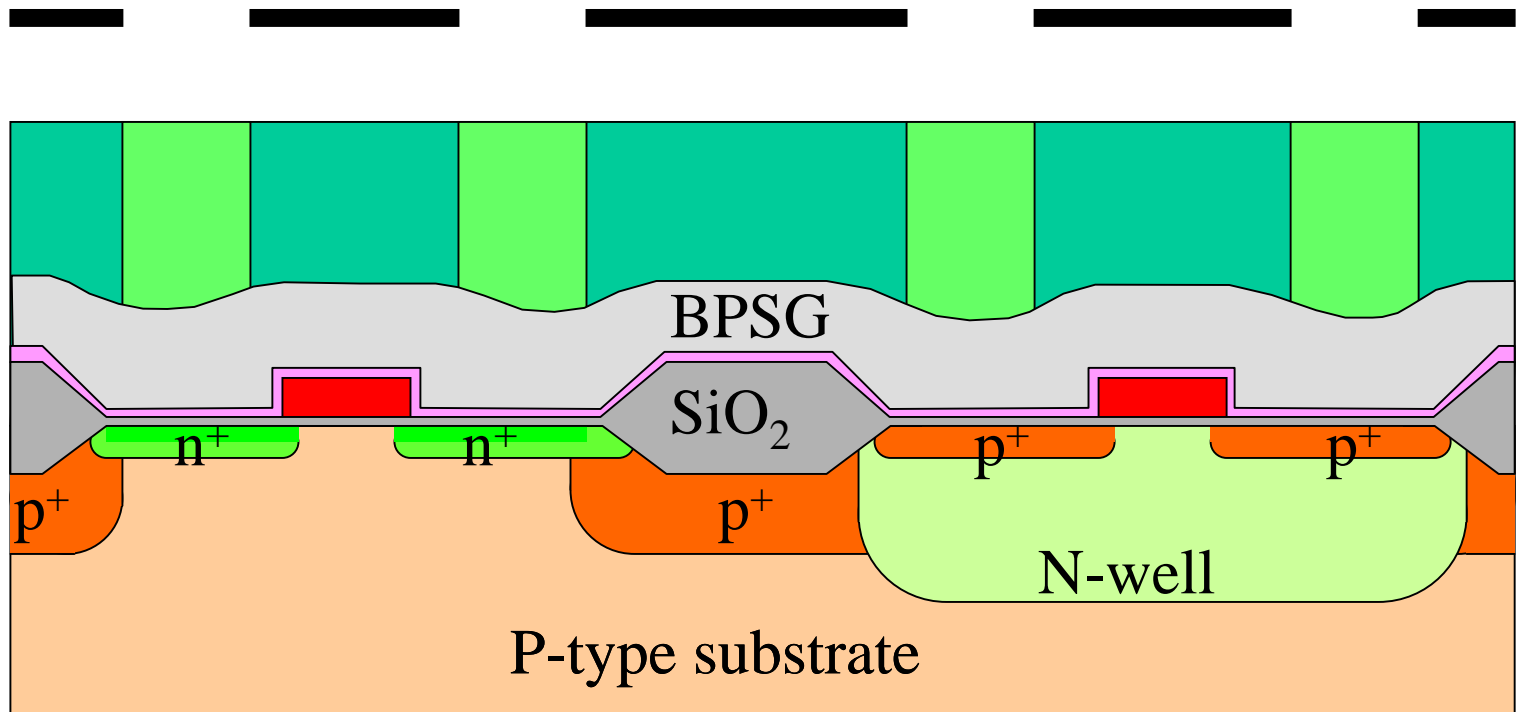
BPSG Reflow



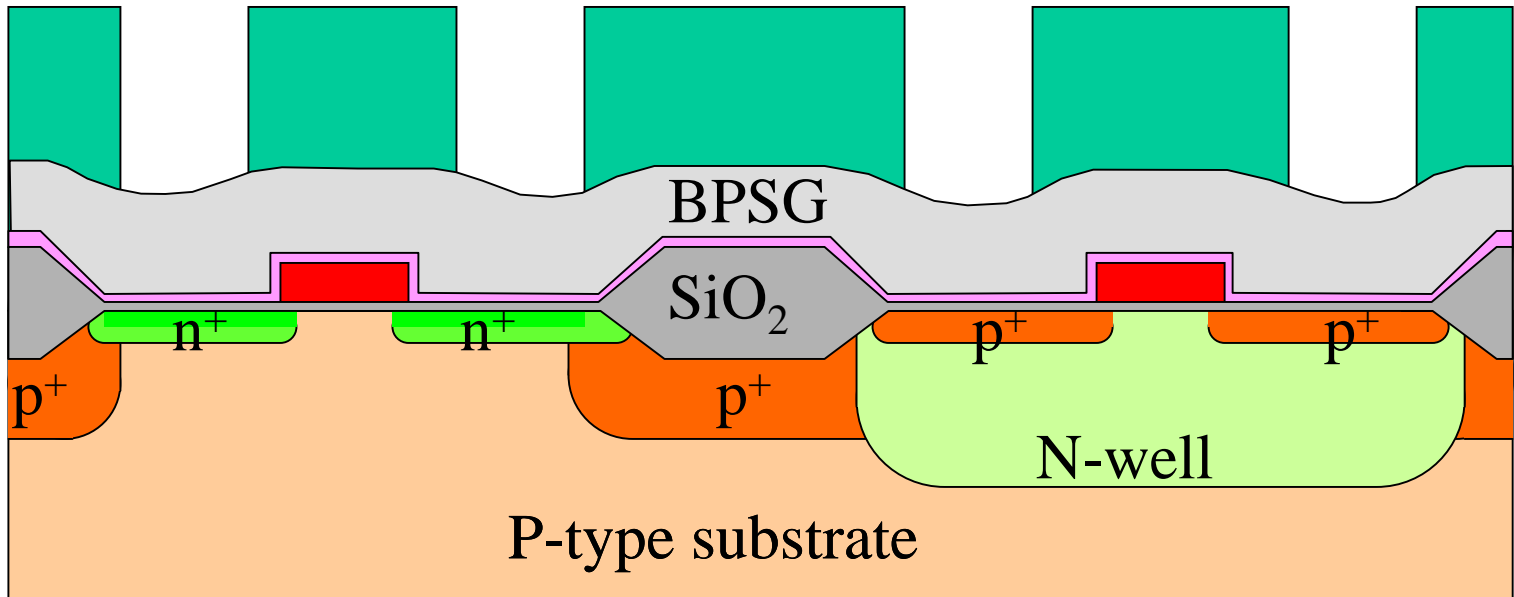
Photoresist Coating



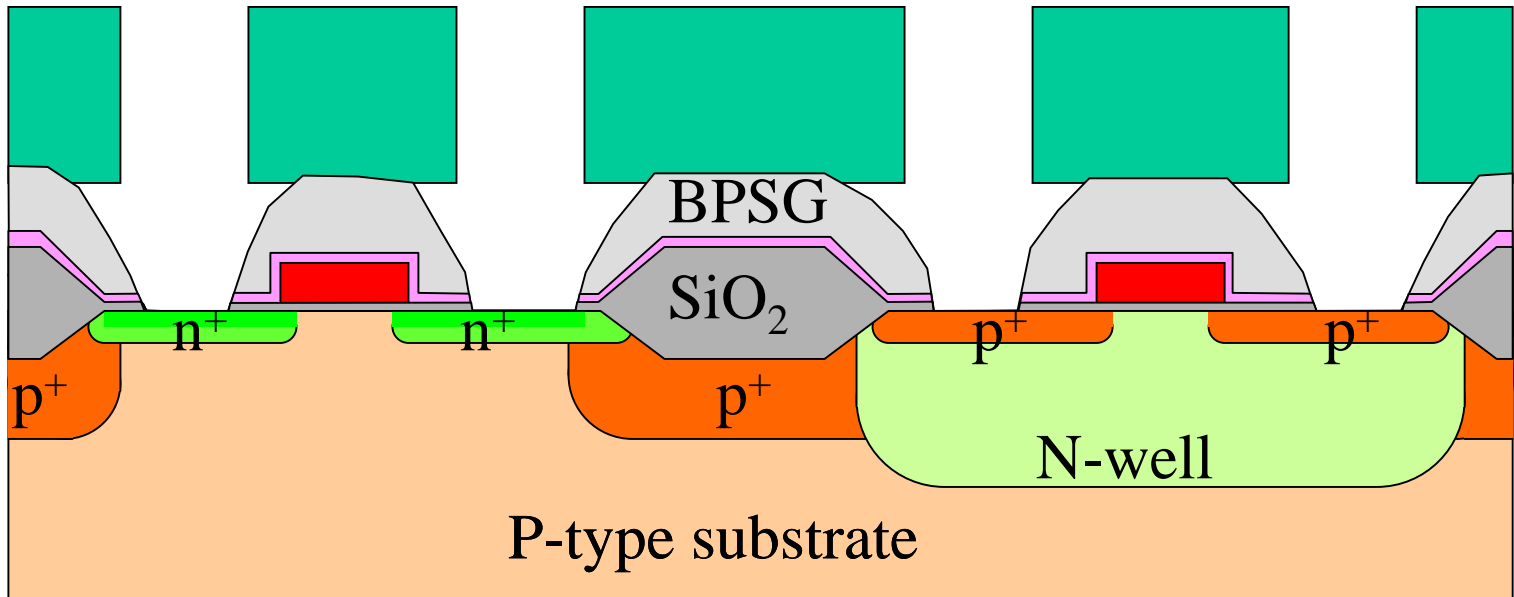
Mask 6 , Contact Exposure



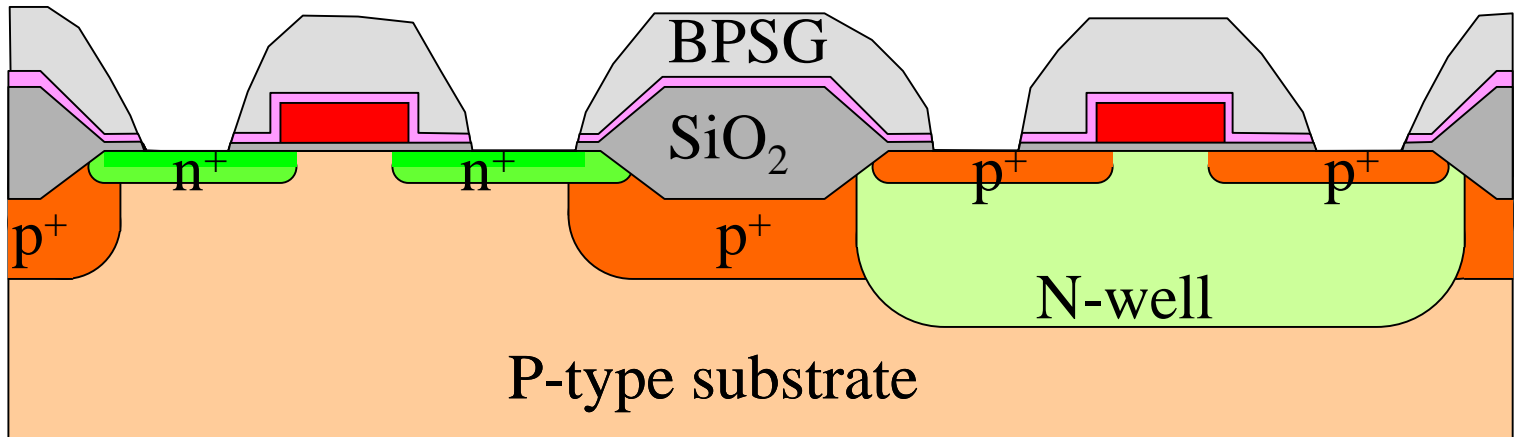
Development



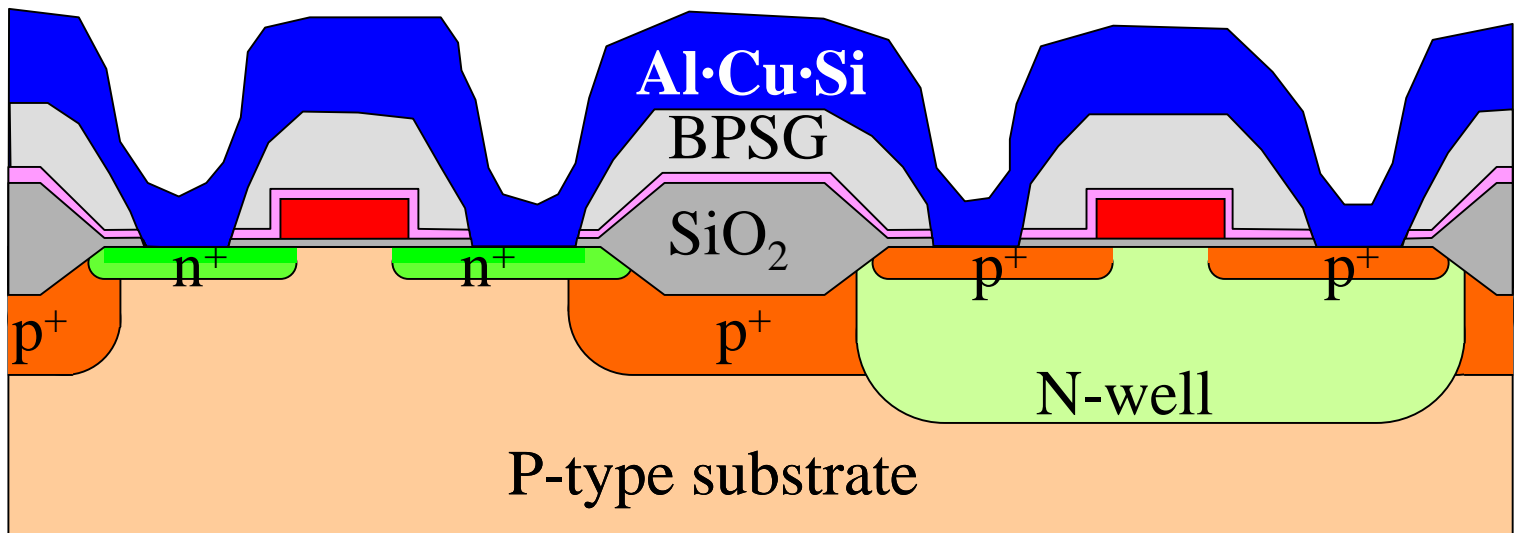
Contact Etch



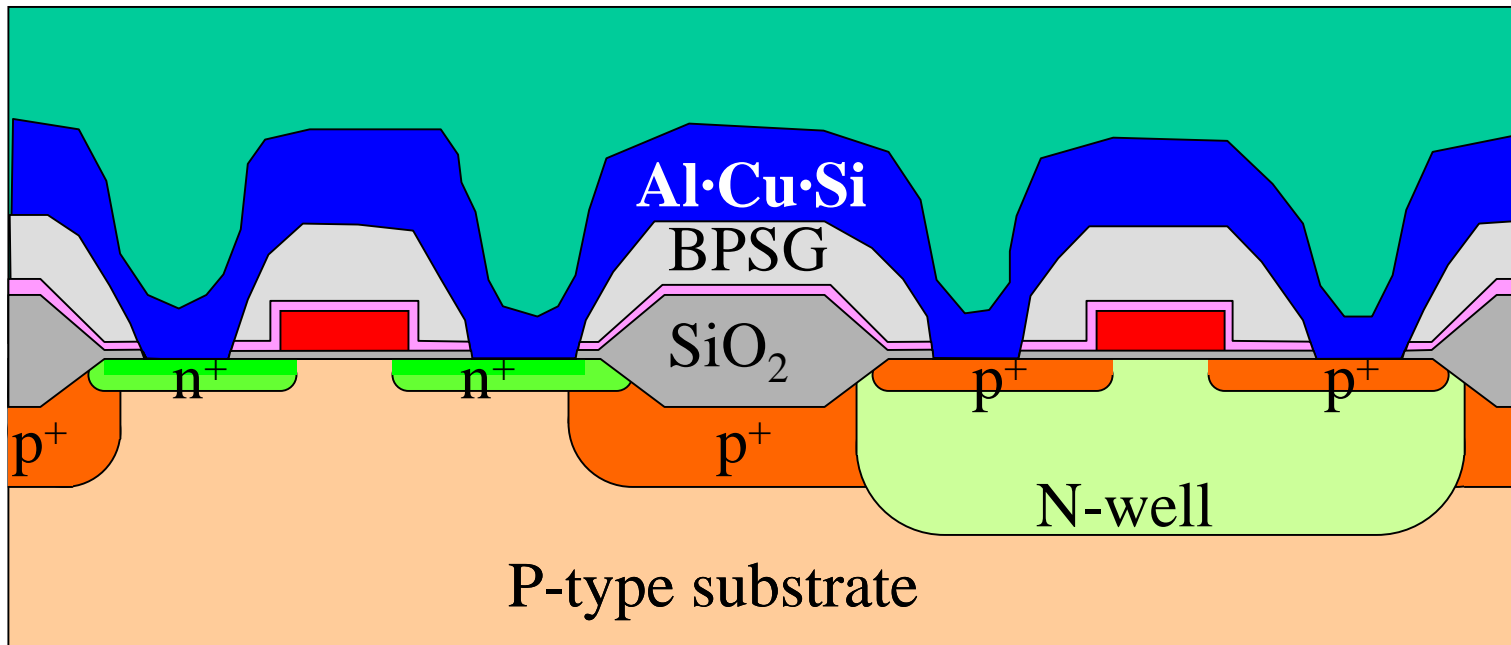
Strip Photoresist



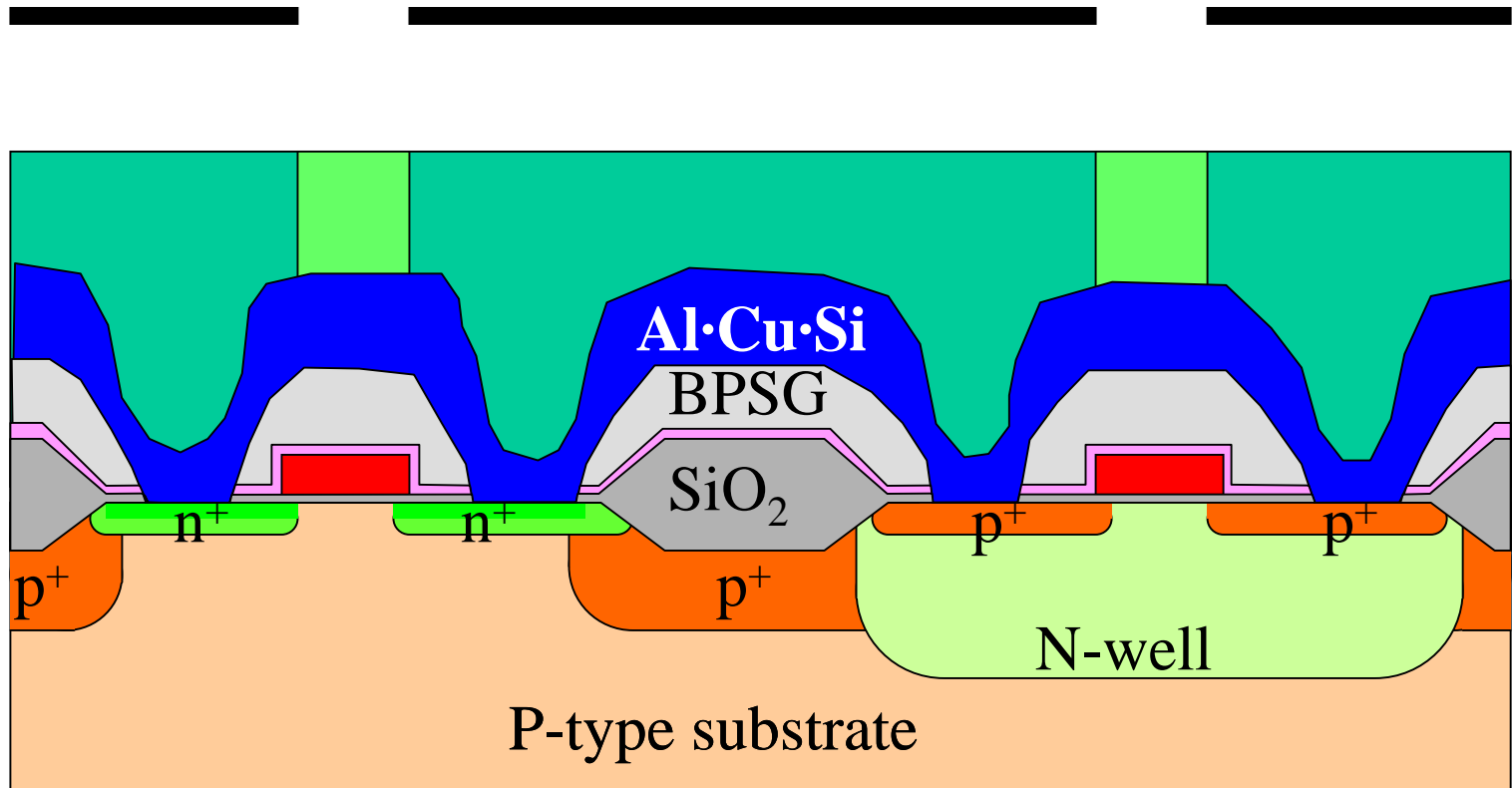
Metal Deposition



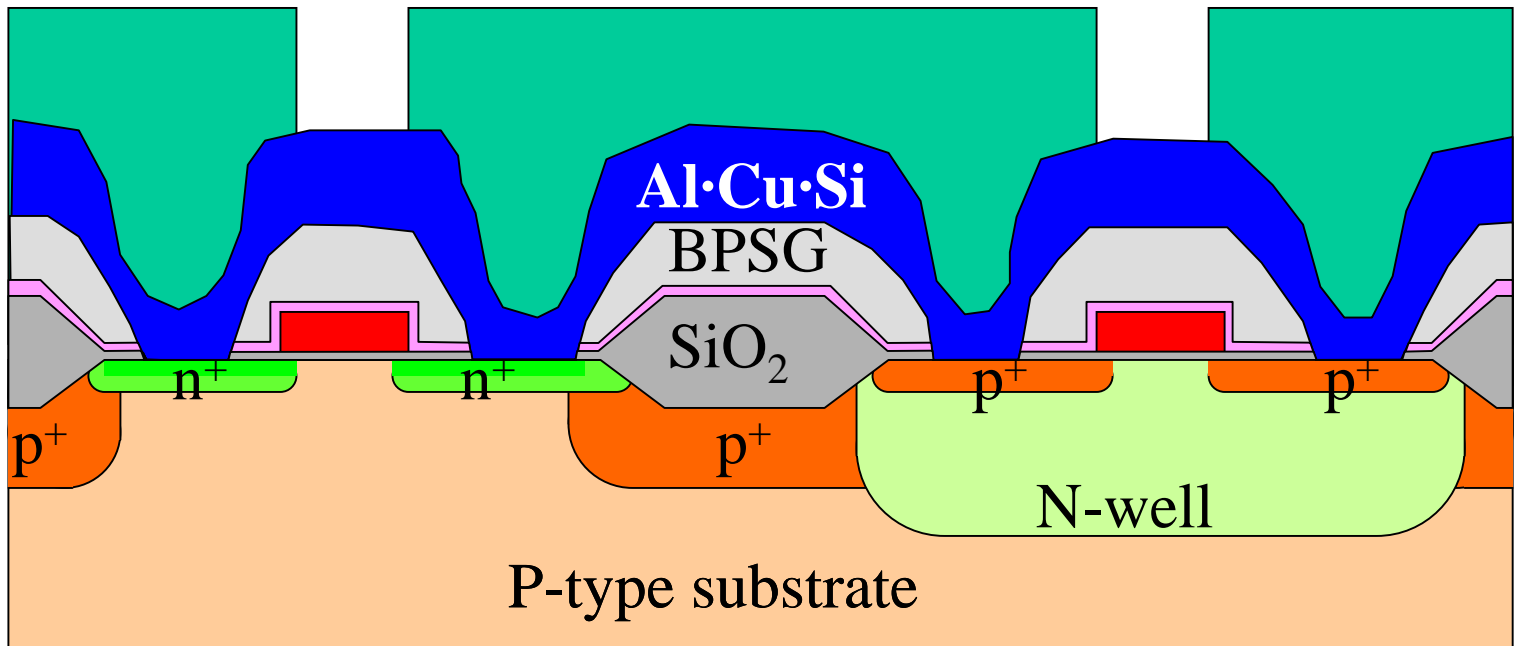
Photoresist Coating



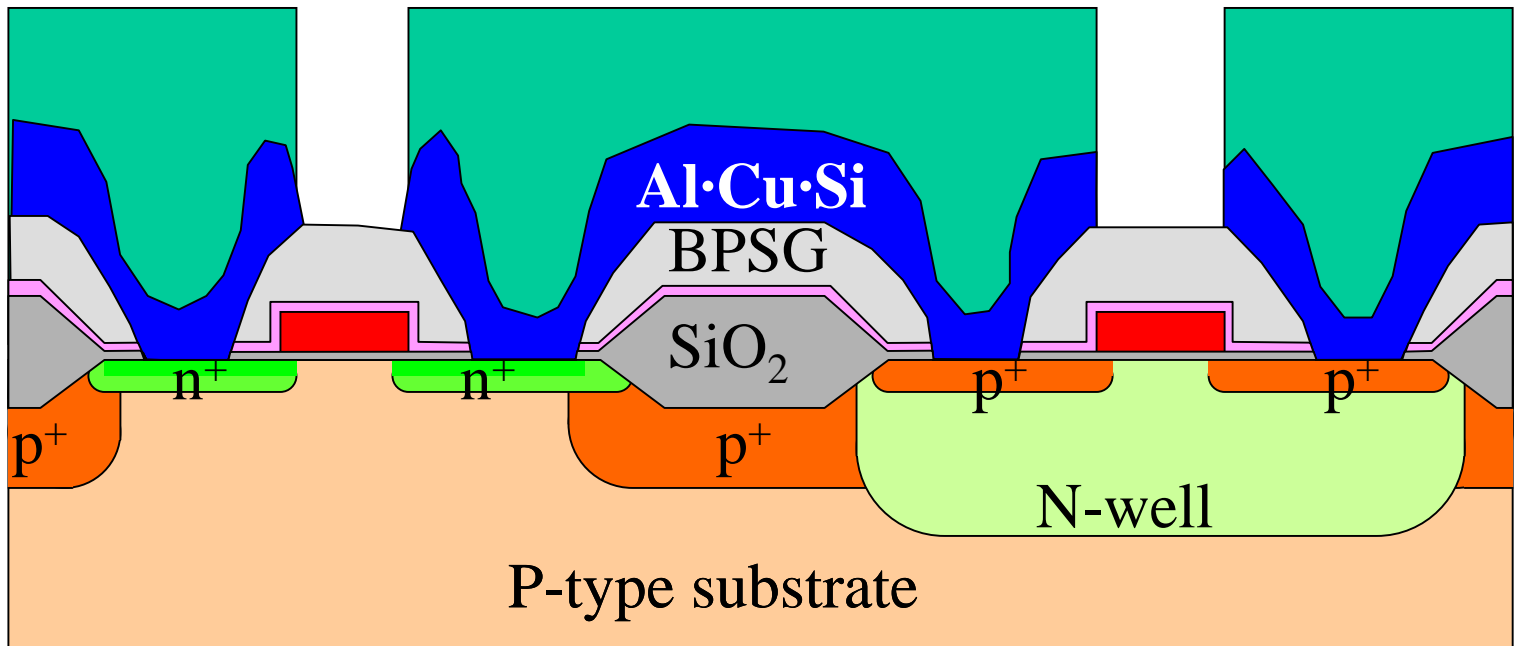
Mask 7 , Metal Interconnection Exposure



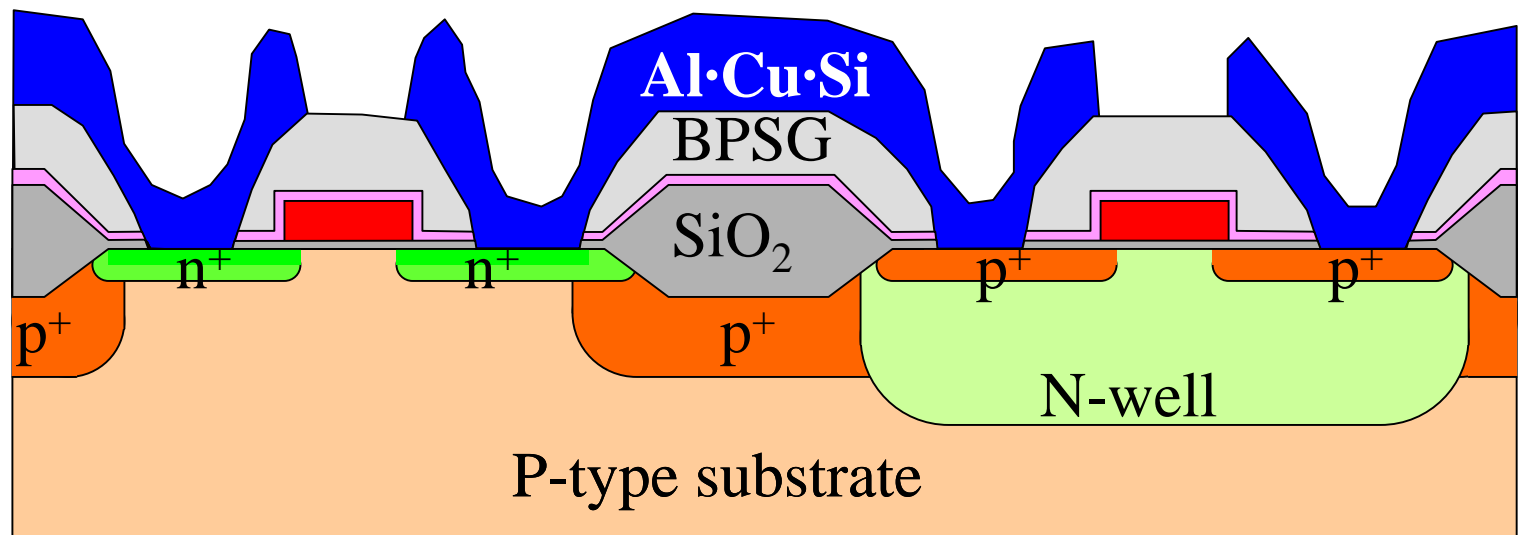
Development



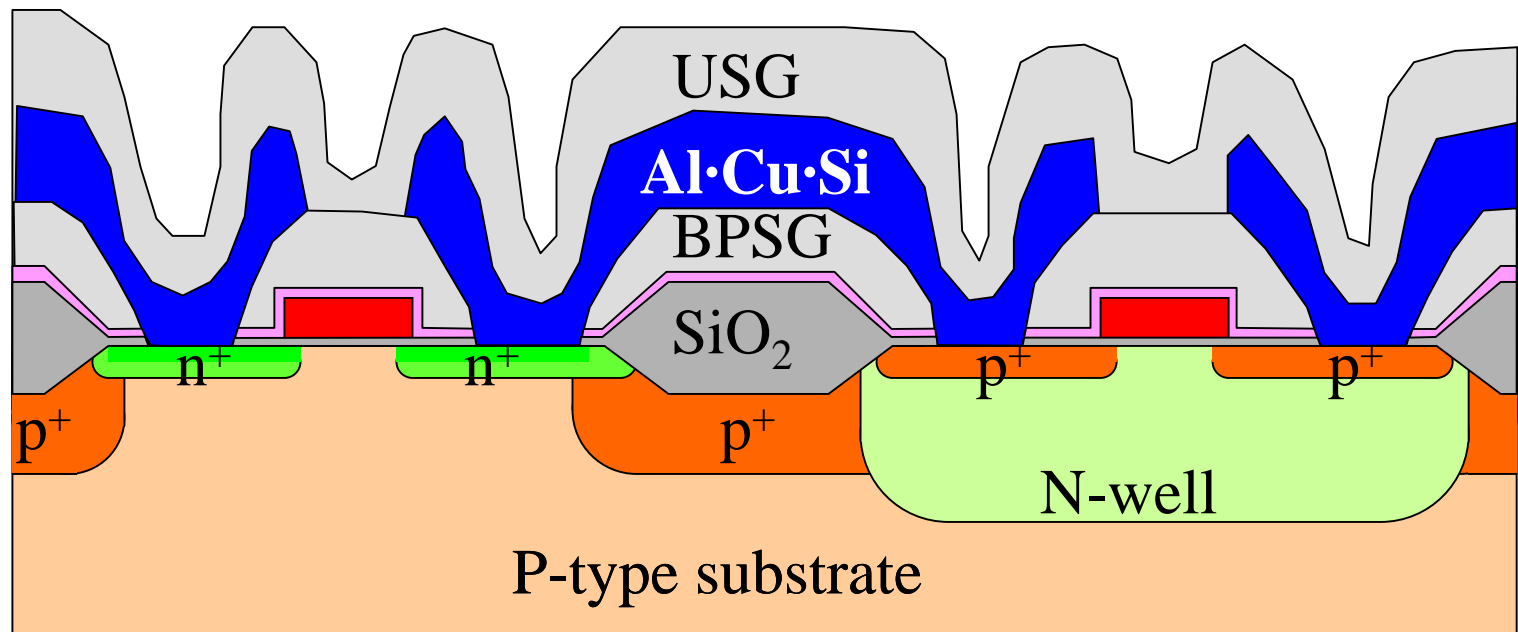
Etch Metal



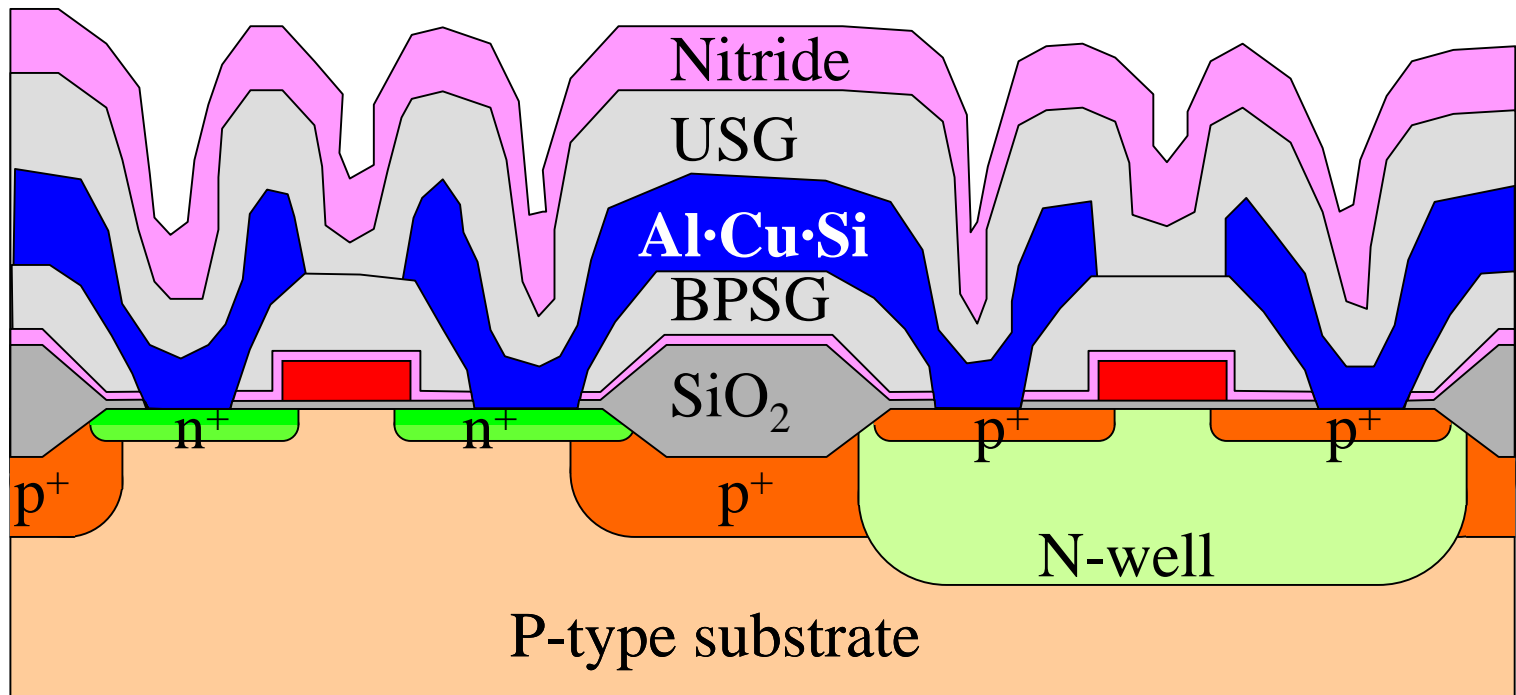
Strip Photoresist



CVD USG



CVD Nitride



IC製程技術導論(III)

- ☒ **NMOS Process Flow及
CMOS Process Flow介紹**
- ☒ **教學成效評鑑**

教學成效評鑑

- (3) 1. 下列哪一個敘述是正確的：
- (1) CMOS比NMOS費電
 - (2) NMOS與CMOS省電能力相同
 - (3) CMOS比NMOS省電
- (3) 2. IC製程中，為了讓晶片表面更平坦以利後段製程進行需要用到何種製程技術？
- (1) 蝕刻製程(ETCHING)
 - (2) 離子植入(ION IMPLANTATION)
 - (3) 化學機械研磨(CMP)
- (2) 3. 在MOS製程中，源極(SOURCE)及洩極(DRAIN)是由哪種製程技術形成？
- (1) 氧化(OXIDATION)
 - (2) 離子植入(ION IMPLANTATION)
 - (3) 化學機械研磨(CMP)
- (3) 4. 在金氧半導體(MOS)中，控制閘通道(GATE CHANNEL)通與不通的是哪一極？
- (1) 源極(SOURCE)
 - (2) 洩極(DRAIN)
 - (3) 閘極(GATE)

教學成效評鑑

- (3) 5. 在半導體工廠中，保持潔淨室(CLEAN ROOM)的潔淨度很重要，若沒有控制好微塵(PARTICLE)，就會掉到生產中的晶圓(WAFER)上，微塵會造成的問題是？
- (1) 產品可靠性(Reliability)問題
 - (2) 產品良率(Yield)問題
 - (3) 以上皆是
- (2) 6. 1微米(1μ) = 1×10^{-6} 米，約為頭髮的？
- (1) 1/10
 - (2) 1/100
 - (3) 1/1000
- (2) 7. 在 N 型金氧半導體(NMOS)中主要傳動的載子(CARRIER)是：
- (1) 電洞(HOLE)
 - (2) 電子(ELECTRON)
 - (3) 中子(NEUTRON)
- (3) 8. 要長MOS中的二氧化矽閘層需用到何種製程技術？
- (1) 擴散(DIFFUSION)
 - (2) 蝕刻(ETCHING)
 - (3) 氧化(OXIDATION)

教學成效評鑑

- (3) 9. 下列製程技術中哪一個的作用類似蓋房子時所用的模板在使用後需要去除掉：
- (1) 金屬化(METALIZATION)中的鋁矽合金
 - (2) 化學氣相沉積(CVD)中的氮化矽
 - (3) 微影術(PHOTO LITHOGRAPHY)中的光阻(PHOTO- RESIST)
- (2) 10. 需要使用光罩(PHOTO MASK)才能完成的製造技術是？
- (1) 氧化(OXIDATION)
 - (2) 微影術(PHOTO LITHOGRAPHY)
 - (3) 化學機械研磨(CMP)
- (3) 11. 一IC具有二千三百萬個MOS元件(電晶體)，請問此IC為下列的那一種？
- (1) 小型積體電路(SSI)
 - (2) 中型積體電路(MSI)
 - (3) 超大型積體電路(VLSI)
- (2) 12. 潔淨室(CLEAN ROOM)裡的環境應儘量保持在下列那一種狀況下？
- (1) 擾流
 - (2) 層流
 - (3) 亂流

教學成效評鑑

- (1) 13. P型半導體內下列那一個陳述是對的？
- (1) 多數載子是(CARRIER)電洞(HOLE)，少數載子(CARRIER)是電子(ELECTRON)
 - (2) 多數載子是電子，少數載子是電洞
 - (3) 電子與電洞數目一樣多
- (3) 14. MOS製程中的氧化(OXIDATION)製程是在下列那一樣設備內完成的：
- (1) 蝕刻槽內
 - (2) 金屬濺鍍腔內
 - (3) 氧化爐管內
- (2) 15. 1nm(Nano Meter，奈米)是幾um(Micro Meter，微米)
- (1) 1/100
 - (2) 1/1000
 - (3) 1/10000
16. MOS的名稱是以元件的結構來命名的，其中M代表METAL，O代表OXIDE，S代表 SEMICONDUCTOR 半導體。
- (3) 17. 一個金氧半導體(MOS)元件可以看成是一個？
- (1) 變壓器
 - (2) 整流器
 - (3) 電子開關

教學成效評鑑

- (2) 18. 矽是生產積體電路很重要的原材料之一，它約佔地殼表面成分的？
- (1) 5%
 - (2) 25%
 - (3) 75%
- (1) 19. 1958年德州儀器公司(TI)的JACK KILBY製造出全世界第一個IC，這個IC是？
- (1) 小型積體電路 (SSI)
 - (2) 中型積體電路 (MSI)
 - (3) 超大型積體電路 (VLSI)
- (3) 20. 最早期金氧半導體(MOS)的閘極(GATE)多用鋁形成金屬閘，現今最常用複晶矽(POLYSILICON)形成矽閘，複晶矽是用何種製程技術完成的？
- (1) 擴散 (DIFFUSION)
 - (2) 化學機械研磨 (CMP)
 - (3) 化學氣相沈積 (CVD)
- (3) 21. 微影製程 (PHOTO LITHOGRAPHY) 的先後次序是：
- (1) 曝光 → 光阻覆蓋 → 顯影
 - (2) 顯影 → 曝光 → 光阻覆蓋
 - (3) 光阻覆蓋 → 曝光 → 顯影

教學成效評鑑

- (3) 22. IC製程後段的鋁矽銅合金導線使用下列何種製程技術完成的？
- (1) 氧化 + 微影製程 + 蝕刻
 - (2) 擴散 + 微影製程 + 蝕刻
 - (3) 金屬濺鍍 + 微影製程 + 蝕刻
- (3) 23. IC製程最後要蓋一層二氧化矽的護層，此二氧化矽是使用下列何種製程技術完成的？
- (1) 離子植入
 - (2) 氧化
 - (3) 化學氣相沈積 (CVD)
- (2) 24. 下列那一樣是目前半導體技術的主流？
- (1) 雙極性 (BIPOLAR) 電晶體
 - (2) 互補式金氧半導體 (CMOS)
 - (3) 真空管
- (3) 25. 積體電路元件內含有鋁、矽、二氧化矽三類材料，下列何種陳述是對的？
- (1) 鋁是導體，二氧化矽是半導體，矽是絕緣體
 - (2) 矽是導體，矽是半導體，二氧化矽是絕緣體
 - (3) 鋁是導體，矽是半導體，二氧化矽是絕緣體